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Aim & Scope

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- Facilitating the exchange of information and ideas among the engineers, Scientists, Researchers and academicians easily.

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Contents

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COMPILER SYNTHESIS OF MULTIPLY ACCUMULATE (MAC) INSTRUCTIONS USING LLVM BACKEND

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ABSTRACT

Multiply Accumulate (MAC) instruction can improve computation speed, especially in operations such as matrix calculations. FPGA-based soft-IP (intellectual property) design such as CPU-IP can be more flexible for special purpose application scenarios. Our laboratory has designed various FPGA-based CPU designs with/without MAC supports. Since this hardware features cannot be directly represented by high-level languages, such as C/C++, a new compiler synthesized for such CPU becomes a must. The authors have chosen LLVM framework to develop the compiler.This approach can help designersautomatically generate or synthesis various compilersfor different CPU architectures with/without MAC. Users are relieved from intensive knowledge of the intricate prerequisites compiler synthesis for adapting MAC instruction supports. After understanding the hardware MAC support mechanism, CPU designers can run the proposed tool to synthesizea MAC-instruction-supporting compiler. After the modified compiler is synthesized, the process can be integrated to the FPGA-based CPU design flowto speed up HW/SW-co-designs. This tool enables users to automate the design process without manually adaptingcompiler for FPGA-based CPU design flow.

Keywords - LLVM, CPU0, Automated Program

I. INTRODUCTION

The pursuit of optimization has been a driving force behind the progress of human society. In this ongoing evolution, instruction acceleration plays an indispensable role. MAC (Multiply-Accumulate) instruction is crucial for accelerating instructions, and a compiler is required for generating these instructions. The compiler's function is to convert codes of various high-level languages into executable code. Compiler design involves complex stages of source code transformationsuch as parsing, optimization, intermediate code generation, and target code generation. However, for those new to compiler design field, this process may seem too complex withsteep learning curve.

FPGA (Field-Programmable GateArray)[1] is a programmable logic device that includes reconfigurable logic units and interconnects, offering flexibility for customization according to specific application needs. The flexibilityallows for the implementation of various CPU architectures, such as RISC-V processor[2],orevenmore application-specifichardware designlike Convolutional Neural Network (CNN) accelerators [3]. These examples illustrate the versatility of FPGAs in meeting a wide range of processing demands. FPGAs also aid CPU designers in debugging and testing various CPU design parameters, such as register size, bus width, special instructions (e.g., MAC, FFT, matrix multiplication [4][5] for computation acceleration, or interrupts for timing acceleration), cache memory size, and pipeline stages. However, after developing several CPU designs, creating a compiler prototype becomes challenging. This paper will discuss strategies for overcoming compiler prototype challenges.

This paper will discuss strategies for overcoming compiler prototype challenges. Our laboratory has also published papers[6] on this topic, including one on implementing CPUs with specific functionalities on FPGAs [6].

The target CPU architecture (called CPU0 [7]) used in this paper is a simple 32-bit processor designed with a focus on simplicity and ease of comprehensionrather than heavily optimized for cost and speed which are common considerations for complex commercial processors.

In recent years, tools and frameworks [8][9] have emerged to tackle the challenge of creating compiler prototypes after the development of various CPU designs. In this context, we have chosen LLVM (Low Level Virtual Machine) [10] as the foundational framework for the compiler in this paper. Itis an open-source project that provides a modular and extensible compiler framework, allowing developers to more easily build and customize their own compilers (e.g., by adding MAC operation acceleration instructions). While these tools offer convenience, developing a compiler with specific functionalities still requires a deep understanding of computer science.

The aim of this paper is to develop a more automated process for generating compilers using the LLVM platform. To achieve the automated compiler generation purpose, leveraging the modular structure of LLVM allows us to develop a process more easily.

And the framework can get higher levels of automations where multiple stages of transformations from high-level language to target code are needed. Thesestagesinvolve automating tasks such as parsing, optimization, and generating intermediate representation (IR) code, which can reduce the learning curve for developers and improves the efficiency of compiler development. Furthermore, the features of the LLVM platform facilitate the creation of diverse backends to meet various requirements.

In terms of selecting a hardware platform, we have opted for FPGA as the development tool. In comparison to FPGAs, ASICs (Application-Specific Integrated Circuits) [11] are fixed-structure chips with a lengthy development cycle and high costs. It is also important to note that ASIC development components are limited by manufacturers, which can make it still more difficult to obtain and use, thereby increasing the development threshold.

To reduce the compiler synthesis process, we are introducing automation techniques for automatically generating TableGen Definition (TD) files defined inLLVM. TD files eliminates the need for users to engage in cumbersome manual writing and facilitates the automated generation of MAC instructions. By using FPGA as a verification and implementation tool, we provide an efficient solution for automatically generating compilers. This allows users to avoid the complexities of researching and writing acceleration instructions. Meanwhile, in our laboratory, we selected CPU0instruction set architecture (ISA) as the compiler backend. This decision aims not only to synergize with existing laboratory research but also to lay the foundation for further expanding functionality.

II. DESIGN AND IMPLEMENTATIONOF MAC INSTRUCTION IN FPGA-BAESD CPU0

A. MAC (Multiply-Accumulate) instructionMultiply-Accumulate (MAC) is a fundamental kernelin Digital Signal Processing (DSP) and computation-intensive architecture. It is an instruction (or operation) that combines multiplication and addition.

This operation is highly valuable in various fields such as mathematical computation, signal processing, and machine learning. In DSP, the MAC operation is commonly employed for computationally intensive tasks such as filtering and convolution.In hardware implementation, the MAC operation is achieved through dedicated circuits for multiplier and accumulator. This can be executed within a single clock cycle, making it an efficient computational operation.

Typically, the MAC operation involves three operands: two input operands and an accumulator, where the two operandsb and c are input operands. When they are multiplied using a multiplication operation, the result is then accumulated into the accumulatora.

Specifically, the mathematical expression for the MAC operation is:

$$a = a + (b * c) \quad (1)$$

However, it will be more flexible, if Equation (1) is expanded to:

$$d = a + (b * c)$$

(result goes to new variable) (2)

B. MAC in CPU0

The LLVM environment we are using is based on the backend of CPU0. In the case where all the functionalities and architecture of the CPU0 backend (without MAC operation) are well-established, we begin to integrate the MAC instructions. The CPU0 ISA can be categorized into three types: L-type instructions, typically associated with memory operations; A-type instructions, used for arithmetic operations; and J-type instructions, usually employed when altering control flow (i.e., branching). Figure 1 illustrates the ISA subdivision of bit fields for each instruction type.

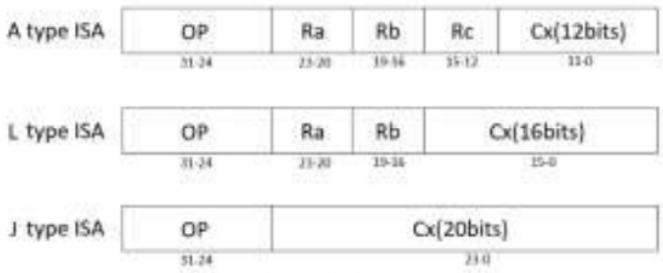

Fig. 1. CPU0 ISA

In this paper, we have introduced a newly devised ISAcalled M-type due to the non-conformance of CPU0's L-type, J-type, and A-type to the format of the MAC instruction. Figure 2 illustrates the subdivision of bit fields for M-type instructions.

As Equation (2), Ra holds the value of operand a, Rbholds the value of operand b, Rc holds the value of operand c, and the final result of the operation is stored in Rd and outputted.

The FPGA implementation of this CPU has been published in [12]. The newly created format can be easily represented as

Fig. 2. CPU0 M-type instruction architecture

In the LLVM CPU0 backend, the TD file defines the instructions, registers, memory layout, and other aspects of the CPU0 architecture. It provides LLVM with a means to translate high-level code into machine code that can run on the CPU0 processor. LLVM offers a set of tools for creating and modifying TD files, including the TableGen tool, which is used to generate code for instruction selection, register allocation, and other compiler optimizations.

The CPU0 TD file serves as an example of the TD files used by LLVM. There are other TD files available for various processors and architectures, and they can be tailored or developed from the beginning as required.C. MAC instruction auto-insertion CPU0 td fileThe modifications of different CPU architecture TD files are generally through manual process.If the process can be automated through an automation script, they can be modified more efficiently without typos or errors. In this paper, the script is defined and processed by a dedicated python program. The first step is to import the user's customized CPU0 instruction file. The Python program will then examine and search for the corresponding TD filesof specific part of these files without modifying any other ill-relevant content. Additionally, it will insert the MAC instruction into the identified TD files. Various TD files serve different functions; for example:

1. `CPU0InstrInfo.td`: This is the primary TD file for the CPU0 instruction set, which includes all instructions of the CPU0 instruction set along with their descriptions.
2. `CPU0AsmParser.td`: This file defines the syntax for parsing CPU0 assembly language.
3. `CPU0InstrFormats.td`: This TD file defines the formats and opcodes for CPU0 instructions.
4. `CPU0RegisterInfo.td`: This TD file defines the register file for CPU0 its their attributes.
5. `CPU0MachineFunction.td`: This TD file defines the machine functions for the CPU0 architecture.
6. In this paper, we will primarily focus on the TD files `CPU0InstrInfo.td` and `CPU0Format.td`.

III. PYTHON ARCHITECTURE

A. Structure

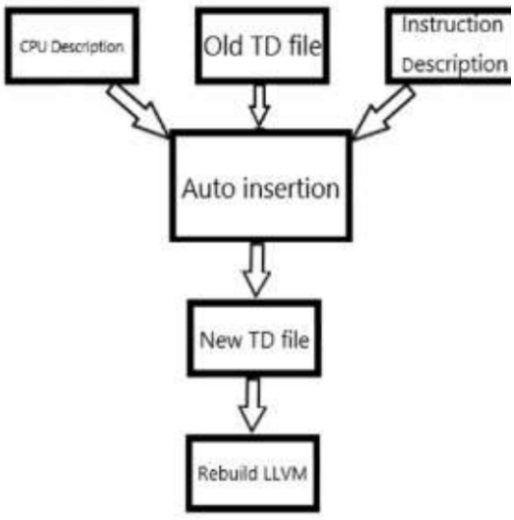

Fig. 3. CPU0 instruction auto-insertion process

Initially, Python will locate the CPU0 TD files based on the file path and add the specified MAC instruction to `CPU0InstrInfo.td` and `CPU0Format.td`. If the TD files already contain MAC acceleration instructions, the program will avoid generating redundant instructions.

IV. RESULTS

After the automatic generation of MAC (Multiply-Accumulate) instructions, the objdump-tool in LLVM can be used to disassemble the machine code into assembly language to verify the presence of MAC instructions. In Figure 4, we have the original C program for Case 1, while Figure 5 shows the disassembly of this C program excluding MAC instructions. Figure 6, on the other hand, illustrates the disassembly with MAC instructions.A MAC operation occurs at PC value 2C, corresponding to the expression "a = a + b * c" in the program. In the red frame of figure 6 The MAC instruction combines theframe of figure 4 multiplication (mul) and addition (addu) operations to enable efficient computation.

```
#include <stdio.h>
int main() {
    int a = 2 , b=2, c=3;
    a = a + b*c;
    return a;
}
```

Fig. 4. Case 1 Original C code

```
Disassembly of section .text:

00000000 /* main:*/
       0: 09 dd ff f0   addiu   $sp, $sp, -16
       4: 09 20 00 00   addiu   $2, $zero, 0
       8: 02 2d 00 0c   st      $2, 12($sp)
       c: 09 20 00 02   addiu   $2, $zero, 2
      10: 02 2d 00 08   st      $2, 8($sp)
      14: 02 2d 00 04   st      $2, 4($sp)
      18: 09 20 00 03   addiu   $2, $zero, 3
      1c: 02 2d 00 00   st      $2, 0($sp)
      20: 01 2d 00 08   ld      $2, 8($sp)
      24: 01 3d 00 04   ld      $3, 4($sp)
      28: 01 4d 00 00   ld      $4, 0($sp)
      2c: 17 33 40 00   mul     $3, $3, $4
      30: 11 22 30 00   addu    $2, $2, $3
      34: 02 2d 00 08   st      $2, 8($sp)
      38: 01 2d 00 08   ld      $2, 8($sp)
      3c: 09 dd 00 10   addiu   $sp, $sp, 16
      40: 3c e0 00 00   ret     $lr
      44: 00 00 00 00   nop
```

Fig. 5. Case 1 LLVM objdump verify result(without mac)

```
Disassembly of section .text:

00000000 /* main:*/
       0: 09 dd ff f0   addiu   $sp, $sp, -16
       4: 09 20 00 00   addiu   $2, $zero, 0
       8: 02 2d 00 0c   st      $2, 12($sp)
       c: 09 20 00 02   addiu   $2, $zero, 2
      10: 02 2d 00 08   st      $2, 8($sp)
      14: 02 2d 00 04   st      $2, 4($sp)
      18: 09 20 00 03   addiu   $2, $zero, 3
      1c: 02 2d 00 00   st      $2, 0($sp)
      20: 01 2d 00 08   ld      $2, 8($sp)
      24: 01 3d 00 04   ld      $3, 4($sp)
      28: 01 4d 00 00   ld      $4, 0($sp)
      2c: 4a 22 34 00   mac     $2, $2, $3, $4
      30: 02 2d 00 08   st      $2, 8($sp)
      34: 01 2d 00 08   ld      $2, 8($sp)
      38: 09 dd 00 10   addiu   $sp, $sp, 16
      3c: 3c e0 00 00   ret     $lr
      40: 00 00 00 00   nop
```

Fig. 6. Case 1 LLVM objdump verify result(with mac)

After successful disassembly, we used the FPGA-based CPU0 simulation tool, which was designed using the Verilog hardware description language, to simulate the results. In the Figure 7 red frame represents the simulation results, where the MAC operation occurs at 4A223400. At this point, R3 is multiplied by R4, and the result is added to R2. The final value observed is 8, which aligns with the expected outcome.

Fig. 7. Case 1 FPGA verify result

Next, we utilized matrix multiplication to confirm whether the designed MAC can be utilized for matrix multiplication, thus reducing computation time. Figure 8 depicts the program for Case 2, which involves matrix operations, while Figure 9 shows the disassembled result. We used the MAC operation to speed up our computations.

```
#include <stdio.h>
int main() {
    int matrixA[2][2] = {{1, 1}, {1, 1}};
    int matrixB[2][2] = {{1, 1}, {1, 1}};
    int result[2][2];

    // Perform matrix multiplication with MAC operation
    for (int i = 0; i < 2; i++) {
        for (int j = 0; j < 2; j++) {
            result[i][j] = 0;
            for (int k = 0; k < 2; k++) {
                result[i][j] += matrixA[i][k] * matrixB[k][j];  // MAC operation
            }
        }
    }
    return 0;
}
```

Fig. 8. Case 2 Matrix Operations Original C code

```
104: 01 44 00 00   ld      $4, 0($4)
108: 09 6d 00 0c   addiu   $t9, $sp, 12
10c: 11 26 20 00   addu    $2, $t9, $2
110: 11 22 50 00   addu    $2, $2, $5
114: 01 52 00 00   ld      $5, 0($2)
118: 4a 35 34 00   mac     $3, $5, $3, $4
11c: 02 32 00 00   st      $3, 0($2)
120: 01 2d 00 00   ld      $2, 0($sp)
124: 09 22 00 01   addiu   $2, $2, 1
128: 02 2d 00 00   st      $2, 0($sp)
12c: 36 ff ff 88   jmp     16777096
```

Fig. 9. Case 2 LLVM objdump verify result

Finally, in Figure 11 of the simulation, the computed result in the red box for matrix multiplication is observed to be 2. The result matches the expected outcome of the C programand the result without macin Figure 10 , where the multiplication of matrices A and B would result in a matrix represented as $\begin{bmatrix} 2 & 2 \\ 2 & 2 \end{bmatrix}$. This aligns with the simulated result.Comparing with the original CPU0 (without mac supporting), the execution time reduces from 830us to 810us. It means 3% efficiency improvement

Fig. 10. Case 2 FPGA verify result(without MAC)

Fig. 11. Case 2 FPGA verify result

The entire process, from inputting the TD file, CPU architecture description, and instruction structure description to generating a new TD file, takes only a few seconds to complete.The manual generation process involves understanding the locations of instruction modifications, testing, and the person making the changes should have a certain level of familiarity with the environment. If done manually in the traditional way, it could take days to monthsdepending on the familiarity of domain knowledge. For a beginner, it might take several times longer (years) to achieve the same results.The proposed method can be of great help to hardware and software engineers. Companies can also be benefitted for human resource reduction.

V. CONCLUSION

In this paper, because of the flexibility of FPGAs, which allow the implementation of various CPU architectures, generating compilers for diverse architectures is not a straightforward task. Therefore, this paper utilizes the instruction set architecture of CPU0. Using Python automation, it generates compilers with MAC instructions and modifies the internal descriptors of CPU0. Executing the Python program streamlines the cumbersome and complex process of manually searching for instructions in descriptor files when making modifications. This significantly speeds up the compiler generation process. Future research could focus on automating various architectures, as the current study only automated the MAC instruction. Alternatively, it could explore the utilization of the M-type instruction set we designed, incorporating additional functional instructions that can be applied universally across different platforms, not limited to CPU0.

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PROBING THE EFFECT OF LENGTH SCALING AND DEFECTS ON THE BEHAVIOR OF HETERO-MATERIAL DOUBLE-GATE TFET BIOSENSOR

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ABSTRACT

In this paper an investigation of the scalability of a hetero-material Double-Gate (DG) Tunnel FET biosensor is made and the intricate features of Trap-Assisted Tunneling (TAT) are explored. To mitigate the unpredictability associated with the process, a dopingless technique to induce p+(source) and n(drain) regions in the TFET structure is employed. However, acknowledging the potential presence of defect(trap) sites in the n-doped strained Si-Ge pocket, a comprehensive analysis is conducted during simulation utilizing specific models. The examination of different trap sites viz. shallow and deep, combined with the assessment of the impact of TAT, reveals that deep traps significantly influence the sensitivity of the biosensor. Furthermore, a study of the scaling capability concerning the gate length, body thickness, and cavity length to evaluate the biosensor's performance is also evaluated. This exploration provides valuable insights into the critical factors shaping the performance and reliability of the proposed TFET biosensor involved in scaling and its implications on the biosensor's performance metrics.

Keywords - Biosensor, Hetero-material Double-Gate TFET, Trap-Assisted Tunneling (TAT), Strained Si-Ge pocket, Sensitivity.

I. INTRODUCTION

TFET is designed to overcome the subthreshold swing (SS) limitations inherent in MOSFETs, with the key goals of achieving lower leakage current levels and a steeper slope. Experimental studies have shown that TFETs can successfully achieve subthreshold swing values (<60 mV/decade) [1-3]. In Conventional Silicon (Si) TFETs, addressing the issue of low ON-current values has spurred researchers to investigate a range of solutions. These solutions encompass adopting highly doped implanted pocket geometry, integrating high-kmaterials, and employing narrow bandgap materials such as III-V semiconductors. [4-6].

Beyond their application in low-power scenarios, TFETs have been considered for biosensing applications. Several studies have explored the potential of TFETs in biosensing, demonstrating their versatility across different technological domains [7-12]. Several factors impact the electrical as well as biological parameters of a TFET biosensor to acquire minimized subthreshold swing (SS), increased ON current, enhanced sensitivity to biomolecules, and decreased exposure to process-induced variations. Our prior research [7], [10-11] has already covered the optimization, fabrication steps analysis, and analytical modeling for the presented TFET biosensor. However, this paper delves into the examination of the impact of potential traps within the n-type doped strained Si-Ge pocket (with 35% Ge composition) of the biosensor while analyzing the scaling of the same.

These traps are anticipated to generate Trap-Assisted Tunneling (TAT) current, a type of leakage current that substantially contributes to parasitic current in TFET devices. These trap states tend to influence the operation of the semiconductor devices during their downscaling which requires exploration.

One demonstrated study [13], has demonstrated that TAT can affect the subthreshold swing and performance parameters of semiconductor devices.

To improve the biosensor's performance parameters, a strained Si-Ge material is used and the composition of Ge (35%) is altered for better results. It has been concluded that a lower bandgap material in the source region with fewer defects can enhance the BTBT rate, thereby reducing the net TAT in the device. Another research work has presented the significance of Si-Ge material and a pocket near the source-channel interface for sensitivity improvement in dielectricmodulated biosensors. It has also provided evidence of the fact that TAT is notably less harmful in tunneling devices due to their different conduction mechanism [14].

There is a notable absence of research and exploration in the domain of scaling capability for dopingless TFET biosensors.Therefore, the foremost objective of this research is to investigate the scaling tendency of the engineered hetero-material double gate TFET biosensor in the vicinity of trap states while maintaining its efficiency. This paper offers an in-depth analysis of how the physical gate length, body thickness, and cavity length influence the electrical and biological performance of dopingless TFET biosensors, specifically focusing on its sensing metrics.

This work is organized into few sections: Section II offers a succinct overview of the biosensor's design and simulation models, with a focus on investigating the scalability in the presence of TAT. Section III delves into the exploration of thedefect sites, and their impact on the sensor scalability. This section also includes a sensitivity analysis of the biosensor, presenting statistics related to ON-current, OFFcurrent, and sensitivity alterations induced by traps. Lastly, in Section IV, the study is concluded by incorporating the potential future avenues for research.

II. DEVICE STRUCTURE AND SIMULATION MODELS

The proposed biosensor employs a dual material double gate-engineered structure with a 2 nm strained Si-Ge pocket, utilizing the dopingless technique to create p+(source)and n (drain) regions. Dopingless technology offers a potential solution to counteract certain limitations stemming from dopant variations in electronic devices, thereby enhancing their performance. In this design, hafnium (with a work function of 3.9 eV) is employed to induce the drain region, whereas platinum (with a work function of 5.93 eV) serves as the source metal, producing a highly doped p+source. The device consists of a 50 nm (Lg) gate portion comprising a dual material gate (tunneling, TG, and auxiliary, AG), as illustrated in Fig. 1(a). The gate-drain underlap length is 22 nm (Lgdu) for leakage reduction at OFF- state. The geometry of the TG is carefully designed to attain improved Vthand ON-current sensitivity.The incorporation of a 2 nm (Lp) strained Si-Gepocket aims to enhance the overall drive current of the biosensor, consequently improving its sensitivity.

The effective oxide thickness beneath the tunneling gate is crucial, particularly as it lies just over the source-channel interface. A minimum nanocavity with a length of 7 nm (Lc) is utilizedto accommodate an adequate number of biomolecule samples and mitigate steric hindrance that could impair the

biosensor's function. The effective oxide thickness is determined according to the guidelines provided by the International Technology Roadmap for Semiconductors (ITRS) for scaling the biosensor.

In our work, various models incorporating Fermi Dirac carrier statistics equations, recombination (SRH), trap-assisted tunneling, concentration and field-dependent mobility,and bandgap-narrowing have been employed. During device simulation for Si and strained Si-Gematerials, the effective tunneling mass of electrons was considered as 0.25 m0;0.55 m0, and for holes was 0.19 m0;1.176 m0[15]. The variation in the tunneling field induced by various traps leads to claims that TFET reliability poses a more significant concern compared to MOSFET reliability. [16]. To account for field and recombination-induced effects on the device performance, the Poole-Frenkel (PF) model is incorporated to monitor alterations resulting from the electrostatic interactions of the defects with the Si lattice, which induce the tunneling with in channel.

While performing the scaling of the proposed biosensor, the effective oxide thickness is determined following ITRS guidelines and ranges from 1.5 to 1 nm, corresponding to gate length variations of 50 to 25 nm in the scaled biosensor. Majorly, the gate length, body thickness, and cavity length scaling are taken into account in addition to the TAT effects. Their impact on sensitivity is evaluated using expressions [7] as:

$$S_{Vth} = \left(V_{th|K>1(bio)} - V_{th|K=1(nobio)} \right)$$
$$S_{ION} = \left(I_{on|K>1(bio)} - I_{on|K=1(nobio)} \right) / I_{on|K=1(nobio)} \quad (1)$$

To verify and validate the presented biosensor, transfer characteristics are calibrated against data from [17].Fig. 1(b) illustrates the good agreement between the calibrated and experimental data for the basic TFET device [17].

III. RESULTS AND ANALYSIS

A. Trap Assisted Tunneling in the proposed biosensor

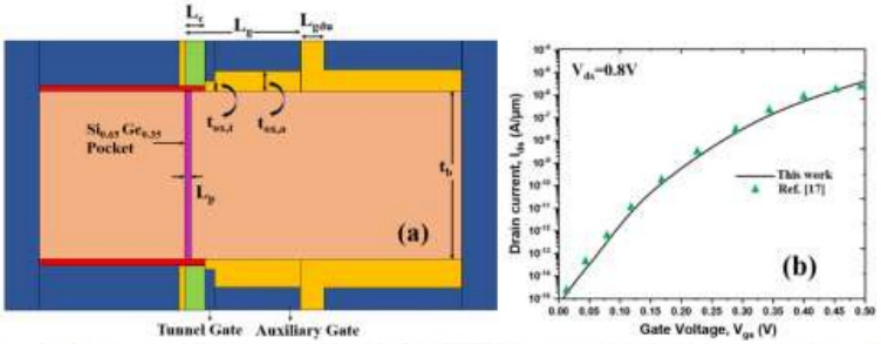

Fig. 1 (a) Schematic of the proposed Hetero-material Double-Gate TFET Biosensor with body thickness (t_b) and tunneling/auxiliary oxide thickness ($t_{ox,t}/t_{ox,a}$) (b) Calibration of the device with experimental data in Ref. [17]

The analysis focuses on potential traps within the doped strained Si-Ge pocket of the proposedbiosensor, which is anticipated to generate a TAT current. This TAT current is,basically a leakage current that plays a significant role in the generation of parasitic current in TFET devices. Collective leakage currents, comprising gate leakage and interface leakage, can significantly mask abrupt variations in the energy bandtunneling current. This leakage is a contributing factor to suboptimal BTBT current values. The presented study investigates the impact of two primary trap states, namely shallow and deep traps, determined by energy levels within the doped pocket. The shallow defect levels are characterized by energy levels situated close to the valence (conduction) band for donor (acceptor) trap entities. Conversely, deep defect levels are located at deeper energy levels (e.g., 0.26 eV), facilitating easier tunneling during the OFF state. [18]. A trap density of ~1022 traps/m2is uniformly applied across all simulations to achieve maximum deviation in the device'selectrical parameters.The biosensor's transfer properties are affected by both shallow and deep sites, as illustrated in Fig. 2(a). Both shallow and deep trap states are expected to have minimal impact on the drive current in an empty (air-filled) and keratin(K=12) occupied cavity. Further, these defect sites affect the leakage current levels, resulting in high IOFFin the device, as seen in the inset of Fig. 2 (a). In particular, the deep defect site causes higher leakage because the impurity energy level of the donor state aligns closely with the channel's conduction band, allowing for quicker electron tunneling from the source to the channel during the OFF state.

In Fig. 2 (b), the ION/IOFF ratio for various biomolecules with TAT is compared. The results indicate a decrease in the ratio with increasing dielectric constant of the biomolecules. This decline is attributed to additional trap states mitigating leakage at low bias, particularly evident in high dielectric constant biomolecules.

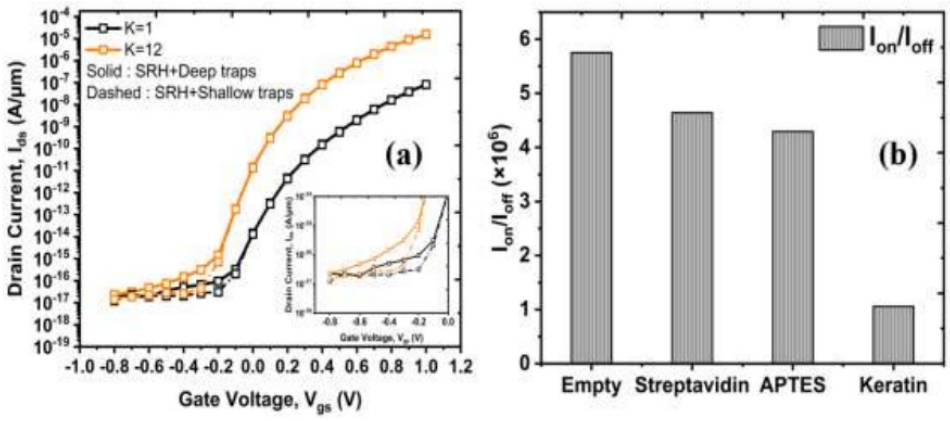

Fig. 2 (a) Transfer characteristics of the presented biosensor for shallow and deep defect sites(b)Assessment ofON-to-OFF current ratiofor different biomolecules in the presence of TAT

B. Device scaling in the presence of traps

When considering scaling, it is essential to refrain from blindly adhering to the scaling guidelines established for MOSFETs. Constant field scaling does not directly apply to the scaling down of TFETs. Hence, constant voltage scaling is used in the presented work.

The influence of reducing gate length (Lg) is illustrated in Fig. 3(a-b). A biosensor must exhibit heightened sensitivity to biomolecule detection and be resilient to inaccuracies arising from dimensional variations. The sensitivity graph illustrated in Fig. 3(a) provides evidence for the feasibility of employing the proposed biosensor at a 25 nm technology node. Particularly, the sensitivities of the on-current and threshold voltage demonstrate significant increases at shorter gate lengths. For a keratin biomolecule at a 25 nm gate length, the proposed biosensor achieves a maximum Vthsensitivity of 542.5 mV, nearly 10 times higher than the ideal Nernst limit.

In Fig. 3(b), as Lgdecreases from 50 nm to 25 nm, there is only a minor change observed in the OFF current and ON-to-OFF currentlevels, which remain well within adequate thresholds. Significantdegradation in these parameters beyond their limits when the gate length reaches 21 nm is observed, indicating that scaling down the biosensor beyond 25 nm leads to unacceptable levels of leakage. This phenomenon is likely due to decreased gate controllability at a gate length of 21 nm. Additionally, a notable increase in substantial leakage at low supply voltage is observed beyond this gate length. As a result, the suggested biosensor can be reduced in size from a 50 nm gate length to 25 nm without sacrificing its sensitivity and electrical performance.

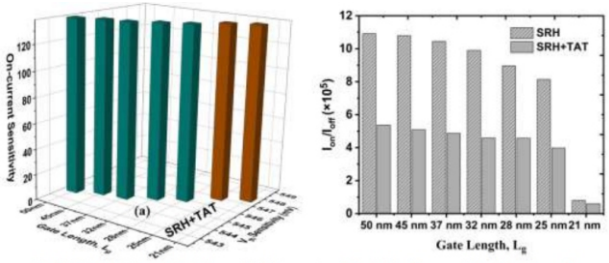

Fig. 3Effect of Gate-length Variation on (a) ON-current and threshold voltagesensitivity (b)I_{ON}/I_{OFF} ratio

The behavior of the TFET biosensor with different body thicknesses (tb) is shown in Fig.4(a-b).A 5 nm thin body generates a high electric field, leading to improvement in ON-current but also causing leakage issues. Consequently, Fig. 4(a) shows a high ON current for tb at 5 nm, but the overall ON-to-OFF current ratio is comparatively lower. The variation in barrier width between Vds of 1 V and 0.1 V implies different leakage current values. Additionally, the reduction in minimum barrier width from 10 nm to 5 nm accelerates drain-induced barrier thinning (DIBT), resulting in an undesired increase of roughly 22.11 mV/V. In The sensitivities tend to diminish with body scaling, posing a potential conflict in which SION decreases while ION grows for a 5 nm body thickness as in Fig. 4(b). The decline in SION can be attributed to the drain current's saturation for K=1. This happens because thinner bodies allow more gate control, causing even an empty cavity to have a high electron drift rate, similar to band modulation at K=12. A similar result is observed for Vth sensitivity as well.

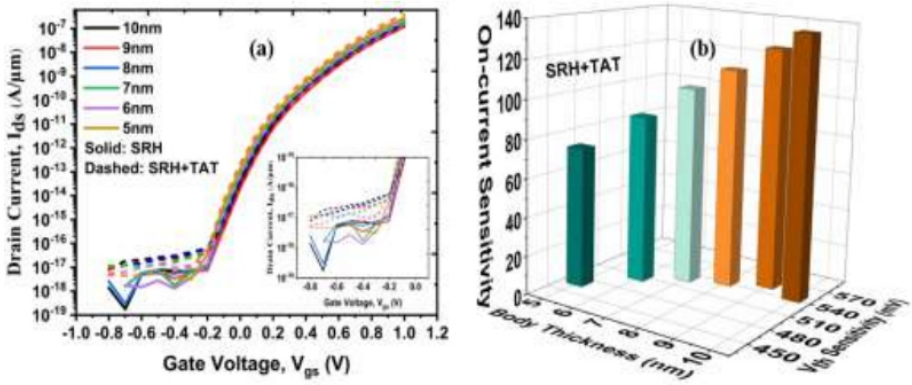

Fig. 4 (a) Transfer characteristics (b) Sensitivity analysis for body thickness scaling in the presence of TAT

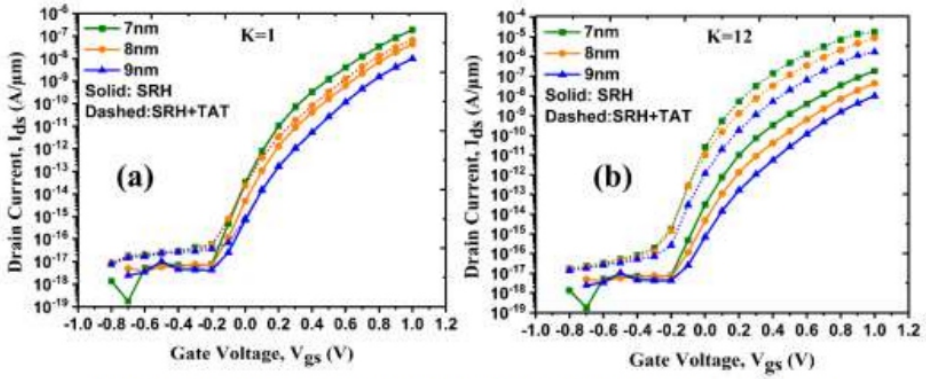

Fig.5Comparison of transfer characteristics for various cavity lengths (a) for K=1 (b) K=12

We examine differences in three cavity lengths: 7 nm, 8 nm, and 9 nm, as depicted in Fig. 5(a) and Fig. 5(b)for K=1 and K=12 biomolecules, respectively. The drain current rises with the dielectric constant (K) as a result of improved gate-channel coupling and the existence of a Si-Ge doped pocket beneath the cavity.It is noted that elongating the cavity length weakens the source-channel interface by increasing the distance between the tunneling gate and it. Consequently, the sensitivity of the on-current decreases with larger cavity sizes.

IV. CONCLUSION AND FUTURE SCOPE

This study explores the impact of length scaling with defects for a hetero-material double-gate TFET biosensor. Deep trap states at a 5 nm body thickness affect sensitivity, increasing Vth sensitivity but reducing ON-current sensitivity. Despite this, the device retains its scalability down to a gate length of 25 nm, a nano-cavity of 7 nm, and a body thickness of 10 nm, while maintaining sensitivity in the vicinity of defects. Essential factors for effectively scaling down biosensors below 50 nm include the ON-to OFF current ratio, drive (ON) current, and sensitivity to the threshold voltage. Performance enhancements are achieved by integrating a counter-doped Silicon Germanium pocket and a high-k oxide near the inter band tunneling junction at the source-channel interface. Non-local BTBT mechanisms and a modified SRH effect enhance simulation accuracy. In the sub-50 nm biosensor with deep TAT, SIon and Vthsensitivity are 1.33×102 and 544 mV. For the 25 nm biosensor, these values remain comparable at 1.37×102and 548 mV, showcasing similar sensitivities despite the downscaling and the presence of deep TAT.

spite the downscaling and the presence of deep TAT. ON-current sensitivity emerges as the most affected parameter when the device is thinned, suggesting that future research should focus on enhancing this metric for improved overall biosensor performance.

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TO OVERCOME ISSUES OF VIBRATION, NOISE AND EFFICIENCY BY ADOPTING BLDC TECHNOLOGIES IN COMMERCIAL APPLICATIONS

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ABSTRACT

Nowadays in every rotary application, electrical motors are used. Earlier, commercial applications commonly used single-phase induction motors, which were generating noise as well as vibrations mainly due to the irregular / uneven torque. For single-phase motor, efficiency is approximately 60-70% at full load. Vibration is generated due to fluctuating stator magnetic field causing irregularities in the torque. This vibration in the single-phase motor leads to generation of noise when operated. Along with it, low PF is of the main causes to impact the Efficiency. On the other side, one must take into consideration its low auxiliary torque and large size of the motor. To overcome the disadvantages of single-phase motors, BLDC (Brushless DC) motors are introduced in commercial applications. BLDC generates constant magnetic field whichfavors in generating the constant torque of the motor. This constant torque reduces vibration as well as noise. Whereas the efficiency of BLDC is roughly in between 85 to 90% with its compact size. This paper mainly focuses on the benefits of BLDC over single-phase motors with respect to vibration, noise, and efficiency. Scalar control and Vector control strategies are used to control the speed of BLDC motors. Considering effective motor controlling strategies, vector control strategies are commonly used though they are complicated.

Keywords - Brushless DC Motor, Single-phase Induction Motor, Power Factor, Field Oriented Control, Integrated Power Module.

1 INTRODUCTION

Single-phase motors are preferred over three-phase induction motors for domestic and commercial applications as they commonly use single-phase supplies. There are some disadvantages to singlephase induction motors with the newly introduced BLDC motor.

II. WORKING PRINCIPLE

The working principles of both motors are different. Single-phase motors work on the single-phase AC power supply, but BLDC motors work on the DC power supply, and that DC supply is given to the three-phase inverter circuit.

Significance of selecting a motor with low vibration and noise levels for improved user experience and reduced wear and tear.

III. OPERATION OF SINGLE-PHASE INDUCTION MOTOR

A single-phase induction motor operates on a similar concept as a three-phase induction motor. To start the three-phase induction motor, we need to connect the three-phase power source to the stator windings. The three-phase power source produces rotating magnetic field in stator windings. Looking into the single-phase motor scenario, the oscillating magnetic field produced in the stator winding. The oscillating magnetic field produces oscillating torque in the rotor. Therefore, the resultant torque generated in rotor is zero.To generate some auxiliary torque in SPIM, we need to generate a rotating magnetic field which is not oscillating.

To produce spinning magnetic field to generate torque in the rotor, we must use another winding in stator which needs 90-degree phase shift. To achieve 90-degree phase shift, we must use Capacitor in series with auxiliary winding. The resultant of these two rotating fields is a rotating magnetic field, which generates torque in the rotor, and the rotor starts to rotate.

But by using the auxiliary winding with the main winding, there will be only a small amount of auxiliary torque generated in the rotor because the magnitude of the magnetic field generated in the auxiliary winding is smaller compared to the main winding, which will not generate a constant rotating magnetic field.

Non-uniform magnetic fields produce non-uniform torque, and due to non-uniform torque, noise will be generated in the motor, which affects auxiliary torque [1].

ΦA = Magnetic field of main winding
ΦB = Magnetic field of auxiliary winding

$$\Phi A = \Phi 1 * \sin \omega t \quad (1)$$

$$\Phi B = \Phi 2 * \sin (\alpha o + \omega t) \quad (2)$$

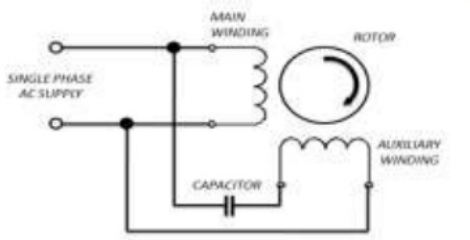

Figure 1. Single Phase Induction Motor stator winding connections

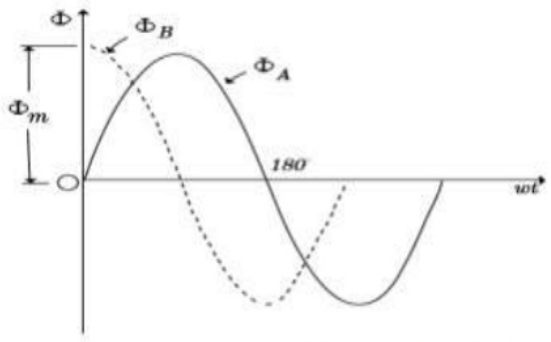

Figure 2. Magnetic field waveforms of main winding and auxiliary winding

Below, Figure (3) shows the necessity of an auxiliary winding in SPIM to generate auxiliary torque. After adding the auxiliary winding with a series resistor, the rotor shaft experiences torque because of the rotating magnetic field.

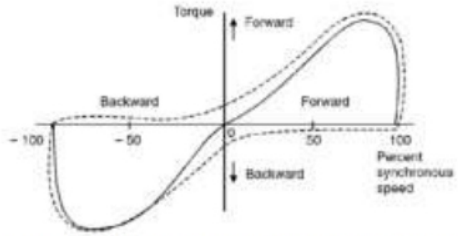

Figure 3. Torque generation in SPIM after activating auxiliary coil.

Demerits of Single-Phase Induction Motor Demerits of Single-Phase Induction Motor Single phase induction motor produces a pulsing magnetic field as a result of the single-phase power source. Variable torque pulses experienced by the rotor as a result of oscillating magnetic field. In a single-phase motor, torque pulses playa major role in generation of vibration in rotor. To provide movement to rotor it's required to add auxiliary winding in the stator. To fulfil the requirement of 90-degree phase shift, it's recommended to sue capacitor in series with auxiliary winding. Capacitor generates phase difference between main winding magnetic field & auxiliary winding magnetic field.

We know that the torque generated in a single-phase induction motor is directly proportional to the resultant magnetic field of the stator winding. In a single-phase induction motor, to maintain a constant magnetic field, an auxiliary winding is present in the motor. The magnetic field generated in the auxiliary winding is 90° behind the magnetic field generated in the main winding. Auxiliary windings contain a winding resistor, winding inductance, and a series connected capacitor. A series-connected capacitor will make the main winding 90° behind the auxiliary winding, and that capacitor is selected while considering the winding inductance and winding resistance of both windings [10]. If the selected capacitor is incorrect or has some tolerance, the resultant magnetic field of the motor winding will not be constant, and the phase difference of the magnetic field of the two windings will be less than or greater than 90°. Consider "α" as the phase difference between main winding and auxiliary winding current. Consider θ as a phase difference between the main winding and the resultant magnetic field.

Consider current flowing through main winding will be IA and current flowing through auxiliary winding will be IB.

From equations (1) and (2), the resultant magnetic field will be:

$$\Phi \vec{}"R"= \Phi \vec{}"A"+ \Phi \vec{}"R"$$

The phase difference (α) of both current windings is important for the resultant shaft torque.
Resultant torque will be,

$$T = K\ IA\ IB \sin(\alpha)$$

Where K is constant

$$T \approx IA\ IB\ Sin(\alpha)$$

Magnetic field generated in the winding is directly proportional to the current flowing through the respective winding.

$$T \approx \Phi 1 \Phi 2 Sin(\alpha),$$

From the above equation, it is observed that torque ripple will be greater if α is less than 90° or if is greater than 90° [17].

The magnetic field generated by both windings, the main winding and the auxiliary winding, will be different. Also, the phase difference between the currents of both windings will not equal 90°. i.e., the stator of a single phase induction motor is generating a rotating magnetic field, but its magnitude will not be constant.

The main parameters behind the generation of an uneven rotating magnetic field will be different magnetic field generation in both windings and phase differences between both winding currents. Main winding and auxiliary winding will not have the 90° phase difference between the current of both windings. 90° phase difference will not be achieved because of the wrong capacitor rating or a poor quality capacitor is used. This results in a reduction in the motor's torque and speed. As this causes an inefficient motor, which causes an under-performing system.

Upon decreased of motor's speed, noise & power consumption gets increased which results down the motor efficiency & also increase motor temperature which reduced motor life.

The power factor of a single phase induction motor is very low, around 0.6 to 0.8. At no load, the power factor will be around 0.20. At low loads, the motor draws more magnetic current, so the power factor will be lower. [17]. At a low α value, each winding will draw current as per the impedance, but the resultant magnetic field will be less than the expected magnetic field. Which results in a lower power factor.One of the reasons for the low efficiency of induction motors is the auxiliary winding [17]. There are two main types of losses present in single phase induction motors. The first is fixed losses, and the other is variable losses. Fixed losses include iron loss (hysteresis and eddy current) and mechanical loss (bearing friction, brush friction, and air friction or windage). Variable losses include I2R loss of the stator and rotor and Stray loss. Because of the low power factor, the motor draws more current, and I2R losses (Copper losses) will increase because of the increased current on the motor, which results in decreasing efficiency of the motor. The efficiency of a single-phase induction motor is 60% to 65% at 75% to 100% load, which is very low [11].

The presence of harmonics in single phase power supply will cause magnetic noise. As harmonic content increases, magnetic noise will increase.

IV. OPERATION OF BLDC MOTOR

BLDC motor controller energizes the stator windings of the motor considering the current rotor position. Hall sensors or Digital encoders are used to detect the exact rotors position. Microcontroller receives data from sensors that track the position of the rotor, but in sensor-less motor control strategy, the back EMF is used to detect the motor rotor position.

Microcontroller gets the rotor position data and other inputs from input signal conditioning & generate PWM pulses to excite the motor winding using switching devices like MOSFETS or IGBT's [5].

BLDC motor controller with position sensor.

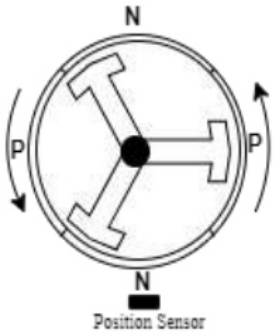

Figure 4. Sensored BLDC Motor with Rotor position sensor

BLDC motor Controller with Back EMF detection

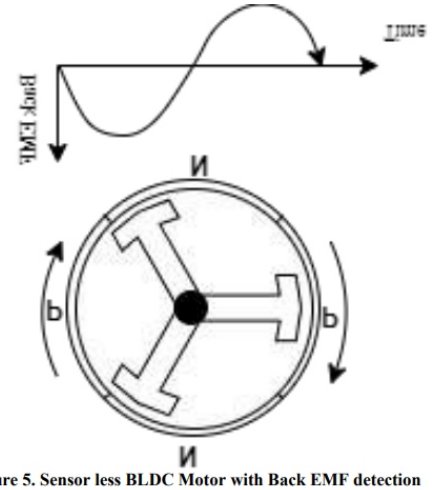

Figure 5. Sensor less BLDC Motor with Back EMF detection

There are two main parts in the BLDC ceiling fan controller: the motor controller section and the power section. Depending on the ceiling fan voltage range, constant DC voltage is generated by the power section. The power section contains the input filter section, rectifier circuit, PFC part, Buck Boost fly back converter, and 12-to-15-volt DC-DC converter, i.e., auxiliary power supply. Initially, MOVs were used with fuse sections for EMI and EMC protection.

Input filter sections are used, which contain capacitors and inductors. After the input filter section, rectification occurs, and after the rectifier, the PFC section is present. Mainly active PFC section used to maintain power factor >0.95. The PFC section contains a fly-back converter or Buck-Boost converter. The output voltage of the PFC section depends on the voltage rating of the BLDC motor. For low-voltage ceiling fans (24 volts), LDO is used to generate the axillary power supply or DC-DC converter used in high-voltage ceiling fans.

The motor controller section contains the microcontroller section, the driver section, the inverter section, the rotor position sense section, etc.

There are four different combinations used for the microcontroller section, the driver section, and the
inverter section.
1. Microcontroller section + Driver Section + Inverter Section
2. Microcontroller section + Inbuilt Driver and Inverter Section
3. Inbuilt Microcontroller and Driver Section + Inverter Section
4. IPM (Integrated Power Module)
5. IPMs are mainly preferred for low-power applications. They have inbuilt intelligence to control the motor, and we need to only tune the IPM as per the motor parameters.

There are two types of ceiling fan motor control strategies to detect the rotor position. One is sensor control strategies, and another is sensor-less control strategies. In sensor control strategies, rotor position is detected by checking the Hall Effect sensor data, and in sensor-less control strategies, rotor position is detected by checking back EMF with ZCD.

In sensor less BLDC motor, rotor position to be detected by using back EMF generates in stator winding. By using back EMF, exact rotor position can be detected. Back EMF produced in stator windings due to present of magnets on rotor. ZCD circuit is used in between back EMF and micro controller as a signal conditioning circuit. Dependingupon the output of ZCD circuit, rotor position detected.

In motor controllers, because of the PFC section, the PF of the controller board is 0.99, near unity [9]. Because of unity PF, the controller board requires less current from the AC power side. The efficiency of the motor is also high compared to a single-phaseinduction motor. Because of the constant rotating magnetic field, ripple torque is not generated on the rotor which had no effect on the vibration and noise. But when the switching frequency is greater than 20 kHz, switching noise will be generated from the inverter section, but the intensity of that noise is very low.

In BLDC motors, we need an extra separate controller to run the motor. Which will excite the winding of the BLDC motor as per referring to the rotor position by taking rotor position data from sensors like Hall Effect Sensors or rotary sensors in sensored control strategies, and by using Back EMF, rotor position is detected in sensor less control strategies [5].

To generate a constant rotating magnetic field, a mainly FOC control strategy is used, which is a more complicated control strategy. In these control strategies, we need to check rotor position using sensors like Hall Effect sensors, encoders, or resolvers, or by using sensor-less control strategies, by using the back EMF of the stator winding, rotor position is calculated or estimated [6]. Also, we need to check the instantaneous magnetic field magnitude and direction. Instantaneous magnetic field magnitude and direction are calculated by measuring the instantaneous current of each phase. By comparing rotor position and magnetic field, depending on the required torque and speed, the next PWM pulses are given to the driver circuit of the inverter and excited the stator windings. All processes are done with the Clark transformation, the Park transformation, and then the inverse Park and Clark transformation [3]. The sampling rate of FOC depends on the PWM frequency. Because permanent magnets are available on the rotor, BLDC motors don't require a separate power source to excite the rotor. Using power electronic devices and advanced motor controlling strategies, motor losses are reduced, which results in increased BLDC motor efficiency. The efficiency of BLDC motors goes up to 90% [14]. Considering the SMPS part, the efficiency of the BLDC motor decreases by up to 75%.

Figure 6. FOC Control strategies flowchart for BLDC Motor controllerGeneral OverviewThe vibration, noise generation, and efficiency of a single-phase induction motor are higher as compared to a three-phase BLDC motor. There are multiple reasons behind vibration, noise generation, and efficiency for single phase motors. One reason is explained in the above section. Because a constant rotating magnetic field will not be generated in the stator of a single-phase induction motor, torque ripple is observed on the motor rotor, which has an effect on vibration and results in noise generation.

As per the available data, noise generation in a singlephase motor for a ceiling fan will be 65 to 80 dB.

While the noise generated by the BLDC motor in a ceiling fan will be between 52 dB and 65 dB, The noise generated by BLDC motors is 50% less than that generated by conventional ceiling fans (single phase induction motors) [8].

The efficiency of a single-phase motor will be 60% to 65% at full load and at 0.6 to 0.7 PF. Also, for the BLDC motor, efficiency will be 74% to 76% at 0.95 PF. This means that with a BLDC controller, we will get more benefits compared to a single-phase induction motor [16].

Compared to BLDC motor, single phase induction motor has rotor losses but in case of BLDC motor such losses not present due to permanent magnets used on rotor, no additional power required to excite the rotor winding of BLDC motor and no power dissipated on rotor.

V. METHODOLOGY

Reasons for noise and vibrations in regular ceiling fans and BLDC ceiling fans:

1. A rotating magnetic field

In ideal conditions, a single-phase motor generates a constant rotating magnetic field. But in practical applications, the resultant magnetic field does not rotate with a constant magnitude.

Because of auxiliary windings, capacitor tolerance and selection of capacitor value. Single phase induction motor consists of two windings, main winding & auxiliary winding. Magnetic fields of the main winding and the auxiliary winding are perpendicular to each other, which is achieved by using capacitor in series with auxiliary winding.

The main winding contains only a resistor and an inductor, but the auxiliary winding contains a resistor, an inductor, and an externally connected capacitor. The capacitor value will be determined by the resistor and capacitor values of both windings.

Because of these, a constant rotating magnetic field will not be generated in a single-phase induction motor, so torque ripples will be observed on the rotor. Because of torque ripples, the rotor will not rotate with constant torque, which results in torsional vibration and then noise [2].

The same laminated stack is used in the stator winding of the BLDC motor. This also causes vibrations, but less than in SPIM.

2. Mechanical ConstraintSPIM The stator and rotor have a laminated core.
Laminated cores are responsible for the generation of noise. Lamination material is made up of magnetic material, like silicon steel. When magnetic material is placed in an alternating magnetic field, it slightly changes shape. This changed magnetic material causes mechanical vibration at 50 Hz to 60 Hz AC power supply.

This generated vibration is transmitted to the surrounding environment through housing, and this causes the noise. This type of vibration is also present in BLDC motors, but only stator lamination is available in BLDC motors, so less vibration is generated. The noise generated by the BLDC motor is negligible.

3. Efficiency
BLDC motors have the same losses, except for rotor losses. Rotor loss also plays a significant role in the efficiency of the motor, which results in an increase in the efficiency of the BLDC motor compared to the single-phase induction motor.

4. Switching frequency circuitry:
Power electronic circuitry wasn't required for SPIM, but to run the BLDC motor, we required power electronic circuitry. These consist mainly of a PFC section, a microcontroller section, and a three-phase inverter section. The PFC section and three-phase inverter section contain high-power switching devices that generate switching noise. Typically, if the switching frequency of the inverter section is more than 20 kHz, switching noise will be generated. Also in the PFC section, in fly-back circuitry, switching noise will be generated in the fly-back transformer and switching device, like a MOSFET. Using goodquality fly-back transformers, noise generation will be reduced. The power MOSFET switching loss will be negligible.

5. Harmonics present in power supply.
The presence of harmonics in input power supply will affect on the performance of motor. When harmonics was present in the power supply of the motor, magnetic noise will be generated.

In Single Phase Induction Motor, we directly connect the input power supply to the motor windings so harmonic frequency power supply will cause magnetic noise.

In BLDC motor because of power electronic components, harmonic content in input power supply is get illuminated so magnetic noise is not present in BLDC motor.

6. Noise testing of conventional ceiling fans vs.

BLDC ceiling fans Here we have checked the noise generated by two ceiling fans. One is a conventional SPIM ceiling fan, and the other is a BLDC ceiling fan. Conventional SPIM ceiling fans were made by Company 1, and BLDC ceiling fans were made by Company 2. Noise was measured by a sound level meter (dB meter). The sound level meter MPN was BandK 2240, with precision class 1. Noise was measured at the midpoint of the blades.

Figure 7. dB meter image

Sr. No.	Parameter	SPIM Ceiling fan specifications	BLDC Ceiling fan specifications
1	No of blades	3	3
2	Air delivery	230 CCM	235 CCM
3	Power	75 Watt	28 Watt
4	Max Speed	380 RPM	340 RPM
5	Sweep	1200mm	1200mm

Table 1. Noise generation comparison for Ceiling Fan application

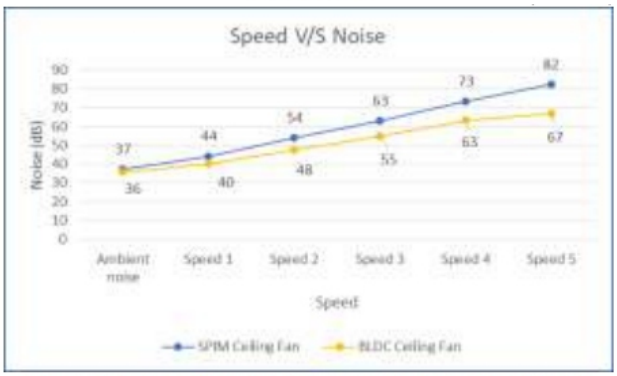

Figure 8. Speed V/S Noise (dB) consumption by SPIM and BLDC ceiling fan.

The above table shows the noise generated by conventional ceiling fans vs BLDC ceiling fans. All the above data was practical data observed in the lab.

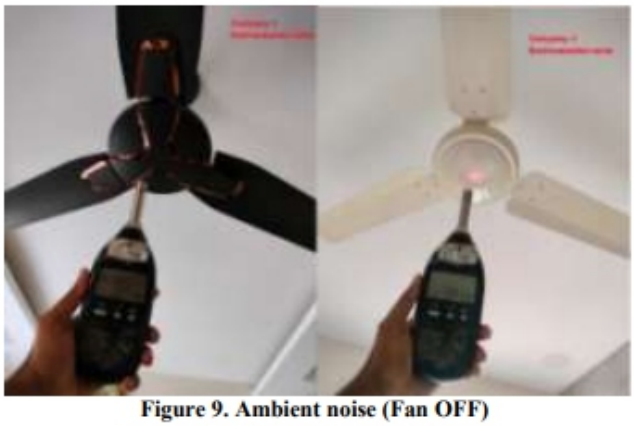

Figure 9. Ambient noise (Fan OFF)

Figure 10. Noise at fan speed 5

VI. ANALYSIS

Sr. No.	Parameter	SPIM Ceiling Fan	BLDC Ceiling Fan
1	Power	75 Watt	28 Watt
2	Air Flow	230 CCM	235 CCM
3	Noise	82.2 dB	66.7 dB
4	Efficiency	60% to 65%	74 % to 76%

Table 1. Different motors parameter comparison for Ceiling Fan application

As per the above table, it shows the comparison study between a convenient ceiling fan and a BLDC ceiling fan. Both ceiling fan generate same CCM and rotate at same RPM where convenient ceiling fan consumes 75-Watt power and BLDC ceiling fan consumes only 28 BLDC motors have low noise (67 dB) and vibration as compared to single phase induction motors (82 dB). BLDC motors have a high efficiency of 75% and a high PF of up to 0.99 compared to single phase induction motors, which have 60% to 65% efficiency and a 0.6 to 0.7 power factor.

We can replace single phase motors with three-phase BLDC motors in all commercial applications. Now BLDC motors are replacing all SPIM in commercial applications like ceiling fans, air conditioners, fridges, exhaust fans, etc. BLDC fans rotate at a constant speed at any input voltage range, but the speed of single phase ceiling fans varies with input voltage. The starting torque of single phase induction motors is very low, and BLDC motors have a high starting torque. A BLDC ceiling fan is more efficient than a conventional ceiling fan.

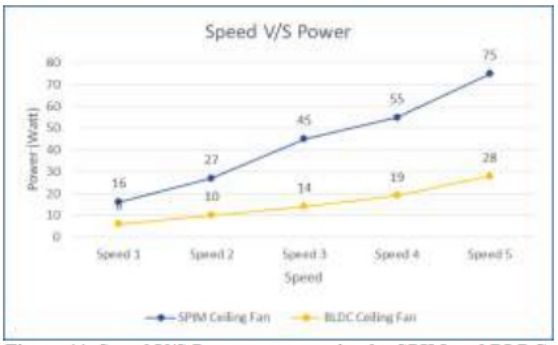

Figure 11. Speed V/S Power consumption by SPIM and BLDC ceiling fan

As per the above table, it shows the energy consumed by an Atomberg ceiling fan compared to an ordinary ceiling fan for different speed ranges [7]. A BLDC ceiling fan saves 65% more energy compared to an ordinary ceiling fan.

As per the above table, it shows the comparison study of the convenient ceiling fan and the BLDC ceiling fan. Both ceiling fans have almost the same air flow. BLDC fans have 235 CCM air flow, and convenient ceiling fans have 230 CCM air flow. The power required to rotate a BLDC fan was only 28 watts with a 67 dB noise level, but a convenient ceiling fan requires 75 watts with an 82 dB noise level.

VII. CONCLUSION

BLDC motors have low noise (67 dB) and vibration as compared to single phase induction motors (82 dB). BLDC motors have a high efficiency of 75% and a high PF of up to 0.99 compared to single phase induction motors, which have 60% to 65% efficiency and a 0.6 to 0.7 power factor. At low speed, Single phase Induction motor will consume 16 Watt of power and other side BLDC motor will consume only 6 Watt of power. As the speed of the BLDC fan increases, the noise level of both the fans will increase but the noise generated by SPIM ceiling fan is more compared to the noise generated by BLDC ceiling fan. Initially, ambient noise is around 35 dB.We can replace single phase motors with three-phase BLDC motors in all commercial applications. Now BLDC motors are replacing all SPIM in commercial applications like ceiling fans, air conditioners, fridges, exhaust fans, etc. BLDC fans rotate at a constant speed at any input voltage range, but the speed of single-phase ceiling fans varies with input voltage. The starting torque of single-phase induction motors is very low, and BLDC motors have a high starting torque.

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DUAL-BAND CIRCULARLY POLARIZED ANTENNA FOR WIRELESS COMMUNICATIONS

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ABSTRACT

P-shaped dual-band circularly polarized (CP) antenna for wireless communications with right-hand circular polarization (RHCP), and left-hand circular polarization (LHCP) is presented in this article. The name of the P-shaped circularly polarized patch antenna is derived from its distinct shape, reminiscent of the letter "P." Currently, utilizing microstrip patch antennas in wireless communication takes advantage of their compact and planar design, facilitating effective transmission and reception of signals. These antennas comprise a radiating patch on a dielectric substrate, accompanied by a ground plane beneath. Their streamlined form and ease of integration render them suitable for a wide range of applications, such as wireless local area networks (Wi-Fi), satellite communication, and mobile devices. The meticulous design of the patch dimensions, substrate material, and feeding mechanism aims to achieve optimal performance. Microstrip patch antennas demonstrate versatility by operating across various frequency bands, including those designated for Wi-Fi (e.g., 2.4 GHz and 5 GHz) and Bluetooth. So, this design presents specific advantages and features that render it appropriate for wireless communication applications, ensuring a suitable axial ratio and necessary gain for achieving desired outcomes. The axial ratio serves as a critical parameter, defining the Ellipticity of the radiation pattern and indicating the antenna's ability to maintain signal polarization during transmission or reception. Additionally, Gain is a crucial antenna characteristic, measures the directive properties of the emitted electromagnetic field. So, optimized electrical volume of the proposed structure is 0.46λ 0 × 0.46λ 0 × 0.02λ 0 at 4.4GHz resonant frequency. The measured -10dB impedance bandwidths are 50.7% and 5.7% for (3.37-5.60GHz) & (10.82-11.46GHz) resonating bands at 4.4GHz and 11.4GHz respectively. The measured 3dB impedance axial-ratio bandwidths for (4.65-5.13GHz) and (11.21-11.52 GHz) bands are 9.7% and 2.7%. Agreement of simulation results with measured results ensure the excellent circular polarization at frequency 4.85GHz and 11.4GHz

Hence, these frequency bands contribute to improved connectivity among devices, whether they are stationary or in motion, when utilizing Wi-Fi technology for establishing connections between smart phone and digital instrument cluster of Motorcycle.

Keywords - Antenna, Circularly Polarized, C-Band, X-Band, Aeronautical Mobile, Satellite Communication

Multipath interferences and polarization losses are two main reasons for reduction of effect of linearly polarized (LP) antennas [1-3]. Circularly polarized (CP) antennas can receive all polarizations with outstanding feature of fairlyconstant signal strength therefore circularly polarized antennas are used for reducing these losses. To design a circularly polarized antenna as compare to linearly polarized antenna is challenge in itself. In simulation environment, axial ratio is one of the important characteristics of circularly polarized antenna. Shape of the radiator, ground and feeding technique plays major role in achieving excellent axial ratio. Demand of compact dual/multiband CP antennas has increased manifolds. Numerous dual/multi band LP/CP antennas have been reported in [4-14] for different applications. Single and dual band circularly polarized antennas for various applications are reported. Tuned strip antenna with F-shaped ground [11], U-shaped patch antenna [12], CPW fed fork-shaped antenna [13], loaded square slot antenna with split ring resonators [14] have been reported to achieve dual-band circular polarization.

Single band circularly polarized antennas are encountered in reported literatures which can cover either C- band or X-band applications. Circularly polarized dual band antenna which can cover both C & X-band in single patch has not been reported yet. A new design of dual band circularly polarized antenna for C & X-band applications is proposed in this article.

Geometrical structure of the proposed design with physical dimensions is shown in Fig.1. Frequency 4.4GHz is used for calculating the physical dimensions and for optimization of the proposed structure. P-shaped radiating patch with defected ground (incorporation of square track, square slot, slit and perturbation stub) is intuitively conceived from the literature and different techniques are used to obtain the optimized results. ANSYS HFSS version 13 is used for design and optimization purpose. The proposed antenna is printed on the FR4-epoxy dielectric substrate having thickness (h) 1.6 mm, dielectric constant (Ɛ) 4.4 and loss of tangent (tan δ) 0.02. Micro-strip feed line (λ0/4 mm) with 50Ω characteristics impedance is used for excitation of proposed antenna. To better understand the behavior of the proposed design, stepwise growth of the proposed design in five different steps are displayed in terms of reflection coefficient, gain and axial ratio. The antenna design-A5 is best suited on the basis of simulated results for C & X- band applications. The geometrical structure with physical dimensions and fabricated photograph of the proposed antenna (A5) are shown in Fig.1 and Fig.2(a-b) respectively. Various antenna parameters such as reflection coefficient, gain, axial ratio, current distribution and radiation pattern have been analyzed in simulation environment. Measurement is done for validating the simulated results.

II. EVOLUTION OF ANTENNA DESIGN

The evolution/stepwise growth (cf. table1) of the proposed design is self-explanatory. Defects created on the ground have been parametrically analyzed to get the optimized dimensions of the antenna and antenna parameters. The effect of square track (2mm thick), inner square slot (16mm×16mm), slit (1mm×24mm) and perturbation (3mm× 8mm) created on the ground from antenna A1-A5 is observed in simulation environment. It is clear from Fig.3(a-c) that antenna A1 does not exhibit resonating band, axial ratio band and gain but by creating square track/defect on the ground of antenna A1 (resulting antenna A2), increment in number of resonating bands are observed. Antenna A2 does not pose sufficient gain within the bands. Change in inductive and capacitive effect of input impedance created by square track/defect is the main reason of change in return loss, axial ratio and gain. Electromagnetic coupling may also be the reason for the change in antenna parameters. A further square slot (16mm×16mm) is etched from the ground of antenna A2 to obtain antenna A3 for improving the gain within resonating and axial ratio bands. Antenna A4 is obtained by introducing the slit (1mm×24mm) in antenna A3 which creates the electromagnetic

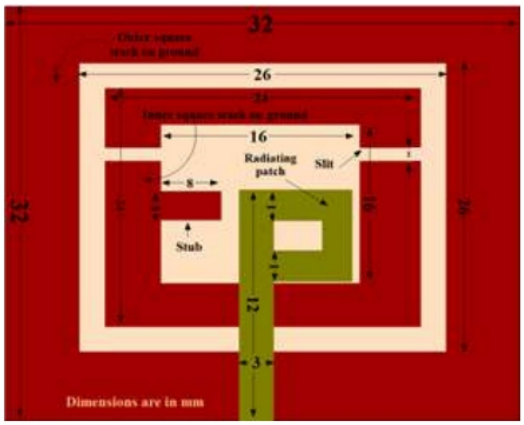

Figure 1: Delay and Area evaluation of an XOR gate.

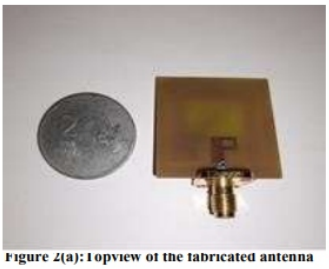

Figure 2(a): Topview of the fabricated antenna

Figure 2(b): Bottom view of the fabricated antenna

coupling gap in the inner ground. Finally, antenna A5 (proposed antenna) is obtained by adding the perturbation in lower left corner of antenna A4. Addition of perturbation alters the electrical conduct of the ground which results in increment in number of resonating bands at higher frequency side. Reflection coefficient, axial ratio and gain of antennas A1-A5 are investigated (cf. Fig.3(a-c)) and tabulated in table 1. It is clear from the table 1 that antenna A5 –proposed structure is resonating with five resonating bands but axial ratio bands (4.65-5.16GHz), (11.19-11.52GHz) lies only in two resonating bands (3.37-5.60GHz), (10.82-11.46GHz) with sufficient positive gain. Therefore, the proposed design (A5) is well suited for C- & X- band applications.

III. RESULT AND DISCUSSION

The proposed design is imprinted on FR4 substrate (cf. Fig.2), and measurement is done for verification of simulated results. Anritsu Vector Network Analyzer MS2038C is used to measure the reflection coefficient (|S11|) and measurement setup used for measurement of gain, axial ratio and radiation pattern of the proposed design is shown in Fig.6. Simulated and measured reflection coefficient and axial ratio of the proposed design is displayed in Fig.4(a). Maximum measured return loss for resonating bands (3.37-5.60GHz) and (10.82-11.46GHz) is -35dB and -18 dB respectively (cf. Fig.4(a, b)).

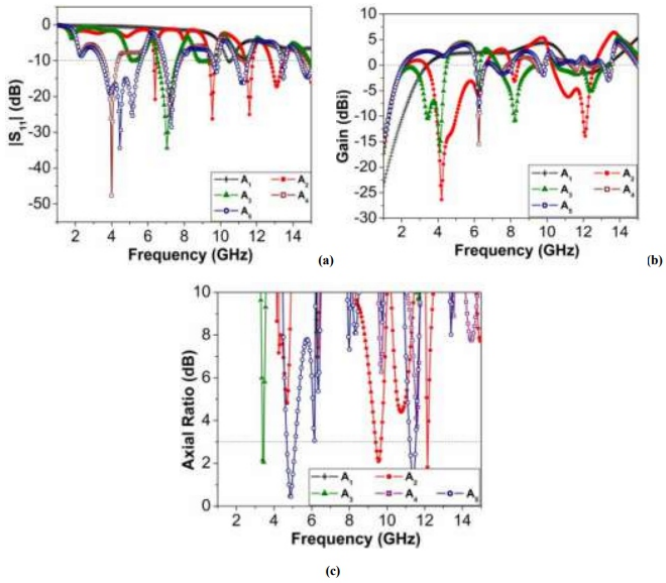

Figure 3: Parametric analysis of antenna (A1-A5) in terms of simulated (a) Return loss (b) Gain© Axial ratio

Measured peak gain for each resonating band is 3.97dBi and 0.96dBi respectively (cf. Fig.4(b, c)). Simulated (measured) impedance axial ratio bandwidth (cf. Fig.4(a,b)) of the proposed design with in axial ratio band is 10.4% (9.7%) and 2.9% (2.7%).

Measurement setup for obtaining the gain, axial ratio and radiation pattern is shown in Fig.6. Simulated and measured radiation pattern for principle planes (x-z and y-z planes) at frequencies 4.85GHz and 11.4GHz are displayed in Fig.5. Bidirectional radiation pattern with right hand circular polarization (RHCP) in +Z direction and left-hand circular polarization (LHCP) in -Z direction is observed from Fig.7. Radiation patterns are little bit distorted from principle axis which may be due to asymmetry in the proposed structure with respect to y–axis. It is clear from Fig.5 that the difference (for both simulated and measured) between RHCP and LHCP component is more than 10dB for both frequencies and planes.

Antennashape (Name)	Resonating bands (GHz)	Gain (dBi)/ frequency (GHz)	Axial ratio bands (GHz)
 (A1)	No band	4.27/9.87	No band
 (A2)	(6.33-6.46) (9.38-9.72) (11.36-11.81) (12.77-13.42)	-1.7/6.46 5.59/9.68 -4.58/11.60 5.69/13.41	(9.43-9.72) (12.1412.17)
 (A3)	(6.52-7.55)	3.09/6.58	(3.34-3.48)
 (A4)	(3.51-5.29) (6.8-7.78)	3.73/5.18 2.50/6.86	No band
 (A5)	(3.37-5.60) (6.89-7.69) (9.62-9.81) (10.82-11.46) (13.36-13.58)	3.97/5.38 0.25/6.89 -0.62/9.62 0.96/11.16 1.46/13.58	(4.655.16) (11.19-11.52)

Table 1 - Stepwise growth and performance of proposed antenna

Simulated surface current distributions at frequencies 4.85 GHz and 11.4 GHz shown in Fig.7 validate the circular polarization of the proposed design. Surface current distributions are simulated using HFSS version 13 from 0° to 270° with advancement of 90°. It is observed from Fig.7 that the direction of surface current reverses when phase changes from 0° to 180° & 90° to 270° respectively. It can also be seen from Fig.7 that X and Y magnitude are almost equal with phase difference of 90° in radiating patch which satisfies the necessary condition for generation of circularly polarized waves. It is confirmed from the Fig.7 that current is rotating in anticlockwise direction and clockwise direction with respect to +Z direction at frequency 4.85GHz &11.4GHz respectively which confirms the RHCP and LHCP waves at frequency 4.85GHz &11.4GHz respectively.

A comparison of previously reported circularly polarized antennas for 4-12GHz frequency range is established in table 2 in terms of electrical size, resonating bands, impedance bandwidth, number of CP bands, AR bands, Impedance ARBW and gain. It is clearly depicted in table 2 that the proposed antenna offers two circularly polarized band with smallest electrical size except [15, 18] whereas other reported antennas offer single circularly polarized band. The reported literatures in table 2 cover only C band applications, whereas proposed design is novel in the sense that it covers C- & X –band with good gain and impedance bandwidth, which is useful for aeronautical mobile, fixed land mobile broad casting, fixed mobile except aeronautical mobile and fixedsatellite or space-to-earth communication.

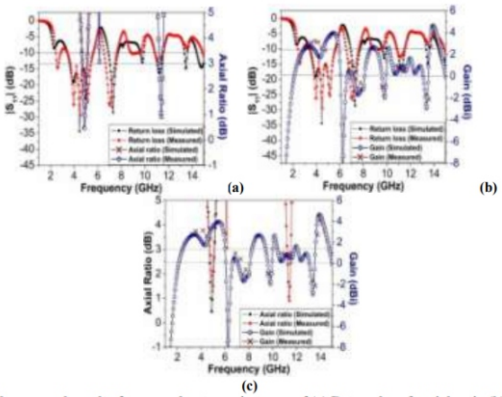

Figure 4: Simulated and measured result of proposed antenna in terms of (a) Return loss & axial ratio (b) Return loss & gain (c) Axial ratio and gain

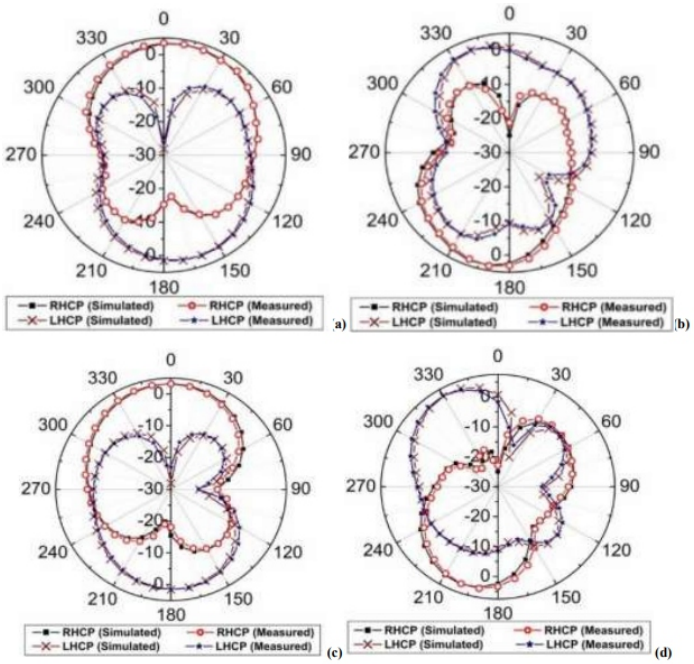

Figure 5:Radiation pattern of the proposed CP antenna in the x-z plane at (a) 4.85GHz, (b) 11.4GHz and in the y-z plane at (c) 4.85GHz (d) 11.4GHz.

Figure 6: Measurement setup for gain, axial ratio and radiation pattern of the proposed antenna in anechoic chamber

Ref.	Electrical size (mm^2)	Resonating band (GHz)	Impedance Band Width (%)	No. of CP bands	AR bands (GHz)	IAR Band Width	Gain (dBi)
[15]	0.33λo × 0.33λo	(4.6–7.5)	2.9/47.9%	1	(4.7–7.2)	42%	6.25
[16]	0.68λo × 0.28λo	(2.11-2.38)/	0.27/12M	1	(5.05-5.56) M	9.6%M	2.15M
		(4.18-4.6)/	0.42/9M				3.42M
		(5.2-5.6)	0.4/8.8M				5.01M
[17]	1.02λo × 0.84λo	(5-7)	2/40%	1	(5-6)	19%	8.9
[18]	0.26λo × 0.26λo	(4.36-7.71)	3.35/55.5M	1	(4.8-7.4) M	42.6%M	5M
[19]	0.54λo × 0.54λo	(3.48-5.86)	2.38/50.9	1	(4.71-5.54) M	16.2%	5.35
[*]	0.46λo × 0.46λo	(3.37-5.60)/	2.23/50.7M	2	(4.65-5.13) M	9.7%	3.97/5.38
		(10.82-11.46)	0.64/5.7M		(11.21-11.52) M	2.7%	0.96/11.16
	[*]- Proposed structure, λo- frequency of operation, M- measured						

Table 2 Comparison of proposed antenna with other reported circularly polarized antennas for 4 to 12 GHz.

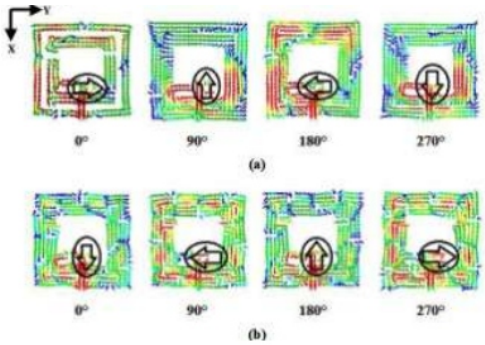

Figure 7: Surface current distribution with 90° phase shifts for (a) 4.85GHz (b)11.4GHz

IV. CONCLUSION

In this paper, the design of novel circularly polarized antenna for wireless applications is presented. Defects (square track, square slot, slit and perturbation) in ground plane is responsible for circular polarization at lower (4.65-5.16GHz) as well as higher (11.19-11.52GHz) frequency bands. RHCP and LHCP waves are offered within 3dB axial ratio bands with measured axial ratio impedance bandwidth of 9.7% & 2.7% at frequencies 4.96GHz & 11.38GHz respectively. Compactness and mentioned characteristics of the antenna makes it suitable for aeronautical mobile (4.65-4.75GHz), fixed land mobile broad casting (4.75-4.99GHz), fixed mobile except aeronautical mobile (5.06-5.25GHz) and fixed-satellite (11.19-11.52GHz) communication.

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