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Contents

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Novel Design Approach of 64-bit Full Adder with Sky130 PDK using Open-Source VLSI Tools

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ABSTRACT

This paper presents the design and implementation of a 64-bit full adder using the SkyWater 130nm Process Design Kit (PDK) and open-source electronic design automation (EDA) tools. The purpose of this research is to develop a highly efficient arithmetic unit suitable for integration in modern digital systems. Utilizing the open-source tools such as Magic-VLSI for layout design, Xscheme and NETGEN for schematic, this paper demonstrates a streamlined design process that underscores the potential of open-source EDA solutions. The designed 64-bit full adder was rigorously tested, and performance metrics were evaluated. The final implementation demonstrated a significant improvement in power efficiency and speed compared to existing designs, with a power consumption of 1.66 uW and a propagation delay of 2.54ns. These results validate the effectiveness of using open-source tools in advanced digital circuit design and highlight the viability of the SkyWater 130nm PDK for high-performance applications.

Index Terms—Arithmetic circuit, Open-Source Tools, Sky130 PDK, Xscheme

I. INTRODUCTION

The increasing demand for high-performance computing has driven the need for efficient arithmetic units, with the 64bit full adder being a critical component. Traditional CMOS design techniques, while effective, often encounter challenges related to scaling, power efficiency, and design complexity. The SKY 130nm PDK along with other open- source tools offers a novel approach by modularizing the design process, enabling more manageable and optimized implementations. When it comes to digital circuit design, creating effective arithmetic circuits is essential for a number of applications, including digital communication systems, signal processing units, and microprocessors. With the use of these circuits, one may perform arithmetic operations on binary numbers, including division, multiplication, and addition. Such a circuit is the adder. An adder is a digital logic that performs addition of numbers and gives output in the form of sum and carry in a binary system. The purpose of this research is Twofold: Firstly, to explore the capabilities of open-source VLSI tools in designing digital arithmetic circuits, and secondly, to provide a comprehensive guide for designing, simulating and implementing such circuits using these tools. Through practical experimentation this research aims to empower individuals interested in digital design to gain hands-on experience with VLSI tools and deepen their understanding of digital arithmetic circuits.

In this research a bottom-to-top approach is adopted to design a 64-bit adder circuit. Beginning at the transistor levelthere is a meticulous construction of the fundamental logic gates required for addition operations, such as NAND gates, OR gates using SKY130 PDK technology. These gates are then systematically interconnected and organized into functional units, following established design methodologies and principles. As ascending through, these units are designed into larger components, culminating in the creation of the complete 64-bit adder circuit. This bottom-to-top approach ensures a systematic and structured development process, allowing for efficient debugging, optimization and scalability while maintaining a clear understanding of the circuit's underlying architecture. By adhering to this method, the author aims to achieve a robust and reliable 64-bit adder design that meets the research's objectives and performance requirements. This study explores the development and application of digital arithmetic circuits that make use of open-source VLSI technology. The objective of using these tools is to comprehensively evaluate the entire design flow, including verifying the layout versus the schematic. The paper not only focuses on the theoretical aspects but also on practical considerations such as performance metrics, area efficiency, and power consumption. Utilizing Magic VLSI for layout design and XSchem for schematic capture, fundamental digital logic gates and arithmetic components like half adder, full adder, 8-bit adder and 64-bit adder are designed.

II. LITERARY SURVEY

Over the years, a number of 64-bit complete adders have been created, including the ripple carry adder, carry lookahead adder, and carry choose adder. Each adder has their own limitations and strengths. For example, Ripple carry adder requires less area for assembling as compared to other adder circuits. On the contrary it shows signified propagation delay making it less suitable for high-speed or large bit-width applications. On the other hand, 64-bit full adder is more compatible and efficient in comparison to other adders as propagation delay is little reduced. 64-bit full adder at 45nm has very low delay as compared to 90nm and 180nm. The author aims to achieve a more compact area i.e, area efficiency, low propagation delay and power consumption. Most papers in literature aim to achieve development in 8bit, 16-bit, 32-bit, 64-bit at different nanometers. The main objective is to design a 64-bit full adder with Sky 130nm PDK using open-source tools. The paper is divided into five sections. Section 3 displays schematic design along with layout designs, section 4 shows the result of the project and section 5 has a conclusion. The following section displays the various open-source tools used in designing of adder, designing rule checking (DRC) along with layout versus schematic LVS) checking methods.

A. Xschem:

XSchem is an effective open-source tool for designing complex digital circuits like a 64-bit full adder due to its robust features, hierarchical design support, and seamless integration with simulation tools. By leveraging these capabilities, designers can efficiently manage and verify large-scale digital designs, ensuring accuracy and performance. The development of a 64-bit full adder in XSchem not only demonstrates the tool's capabilities but also Provides a solid foundation for further digital design projects.

B. Magic VLSI:

MAGIC VLSI provides a modular framework that simplifies the design of complex VLSI circuits. This

section elaborates on the design process of the 64-bit full adder, detailing the key components and their integration. MagicVLSI is an open-source layout tool used for designing integrated circuits (Ics). It provides a versatile environment for creating physical layouts of digital, analog, and mixedsignal circuits. Magic VLSI offers advanced features for editing, viewing and verifying layouts including support for complex geometries, DRC (Design Rule Checking) and LVS (Layout vs. Schematic) checks. It supports various input and output formats, facilitating interoperability with other EDA tools. Magic VLSI is widely utilized by IC designers, researchers and students for its robust functionality and accessibility.

C. Netgen:

Netgen is an open-source tool used for digital net-list comparisons, verification, and conversion. It accepts variousnet-list formats and provides functionalities like net-list comparison, equivalence checking and net-list conversion between different formats. VHDL or Verilog are examples of hardware description languages (HDL) that are used to define 64-bit complete adders. The HDL code is synthesized to generate a netlist. It is used to compare the synthesized netlist against the expected logical structure to ensure that the synthesis process has not introduced errors. It can also translate the netlist into different formats required for various simulation and verification tools. Net-gen is commonly used in both analog as well as digital design flows for verifying the correctness of synthesized net-lists.

D. SKY-130 PDK:

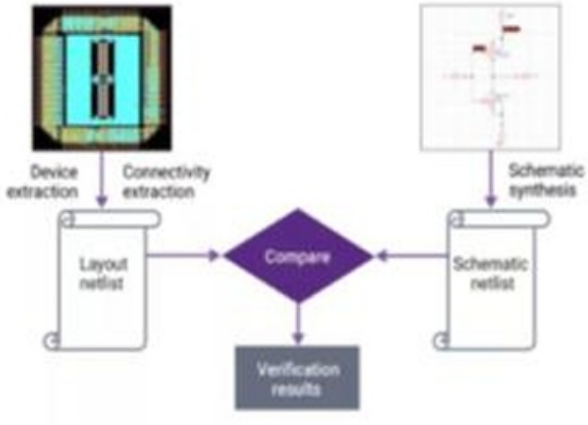
The SKY130 Process Design Kit (PDK) is an essential resource for designing integrated circuits (ICs) using the SkyWater Technology Foundry's 130-nanometer (nm) CMOS process. This PDK is comprehensive, offering a wide range of tools and data necessary for the design, simulation, and fabrication of silicon chips. It supports a variety of applications, including mixed-signal, RF, and analog designs, alongside digital logic. Key features of the SKY130 PDK include Design Rule Check (DRC) to ensure adherence to manufacturing constraints, Layout Versus Schematic (LVS) verification for matching physical layouts to schematic designs, and Parasitic Extraction (PEX) for accurate postlayout simulation and performance prediction. Additionally, the PDK provides standard cell libraries, analog and mixedsignal components, process design rules, and detailed simulation models, ensuring robust and efficient design processes.

Design Rule Checking (DRC):

Design Rule Check (DRC) is a critical process in the field of electronic design automation (EDA) that ensures the manufacturability and functionality of semiconductor devices and printed circuit boards (PCBs). DRC is important because it may identify problems with designs early on, which lowers the possibility of expensive mistakes occurring during manufacture. Typically DRC defines rules based on manufacturing capabilities & limitations. The EDA tools applies these rules to the design layout. Further the violation is detected and reporting is done along with their precise location and nature. In continuation violations are reviewed and corrected. Similarly the SKY130 PDK includes rule decks compatible with industry-standard DRC tools, enabling designers to perform comprehensive design rule checks and ensure compliance with Sky-Water's manufacturing requirements.

Layout Versus Schematic (LVS) Checking:

The interplay between schematic and layout design is critical. The layout must accurately reflect the schematic to ensure the fabricated circuit performs as intended. Discrepancies between the schematic and layout can lead tofunctional failures or suboptimal performance. Layout Versus Schematic (LVS) checks are performed to ensure the layout matches the might require revisiting the schematic to account for parasitic effects and other physical considerations.



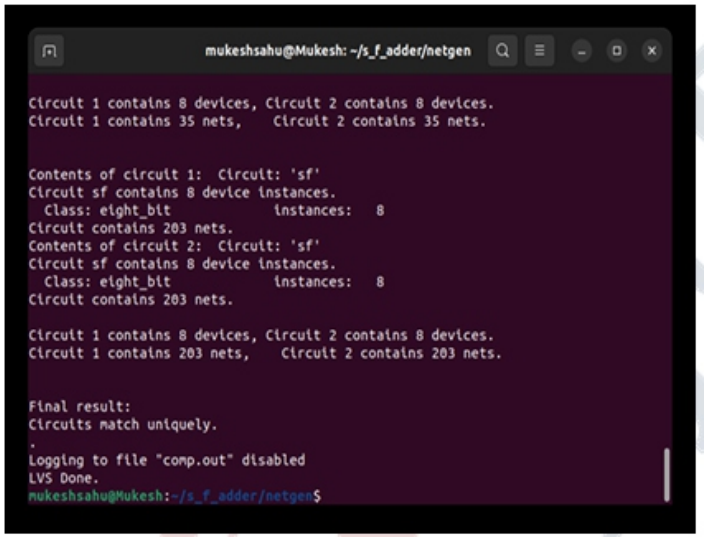


Fig.1.1 LVS for 64-bit adder

III. SCHEMATIC DESIGN FLOW FOR 64-BIT ADDER ALONG WITH LAYOUT DESIGNS

The following is the general workflow for layout design:
• Using the eight-bit adder components in Magic VLSI, design an architecture for a sixty-four bit adder. Arrange the Eight Bit Adder in the active region in accordance with the Sixty Four Bit Adder scheme.
• Ensure that the transistors are positioned correctly and have adequate space between them to prevent interference and ensure proper performance. Utilize metal layers to establish connections between the Eight Bit Adder layout's component parts. To link the transistors' gate, source, and drain terminals, route metal traces in accordance with the schematic design.

• Use Layout vs. Schematic (LVS) and Design Rule Checking (DRC) checks to ensure functional correctness and adherence to design requirements.

Basic Design of Logic GATE:

Logic gates are the building blocks of digital circuitry. Every logic gate performs a basic logical function based on Boolean algebra by operating on one or more binary inputs to produce a single binary output. NAND and OR gates are employed in this situation. A NAND only generates a high output when any gate's input terminal is low. Figure From x to y, which follows, illustrates the schematic, symbol, and arrangement of the NAND gate.

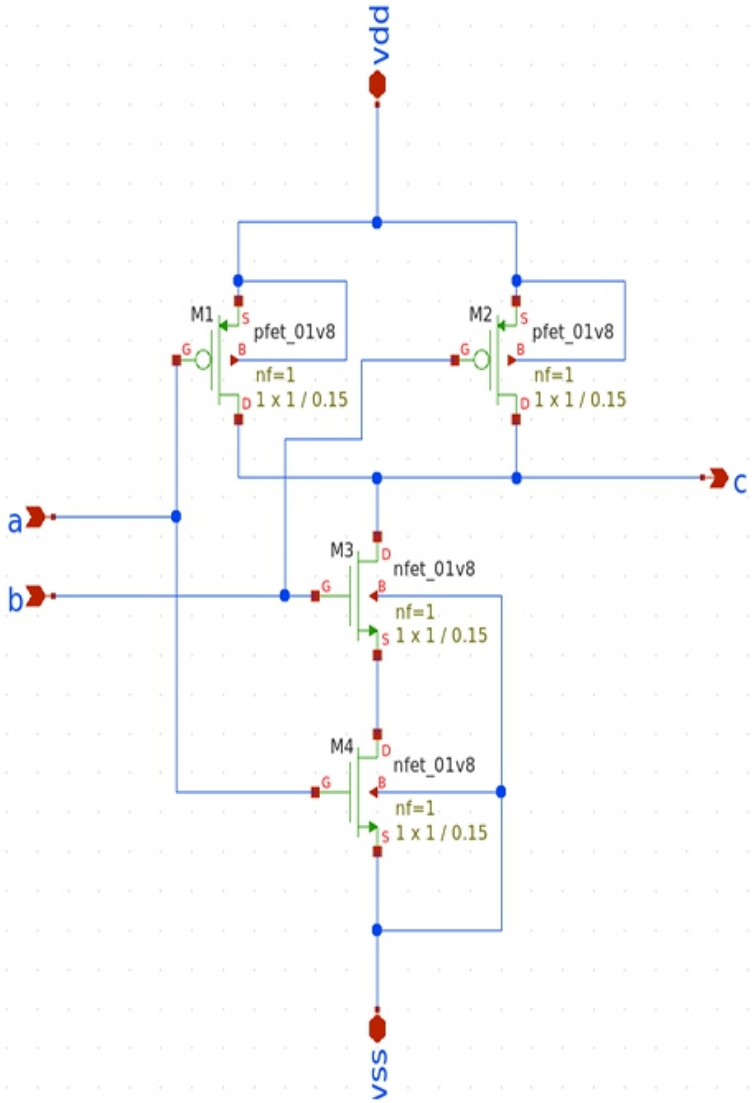


Fig. 1.2 NAND Gate Schematic

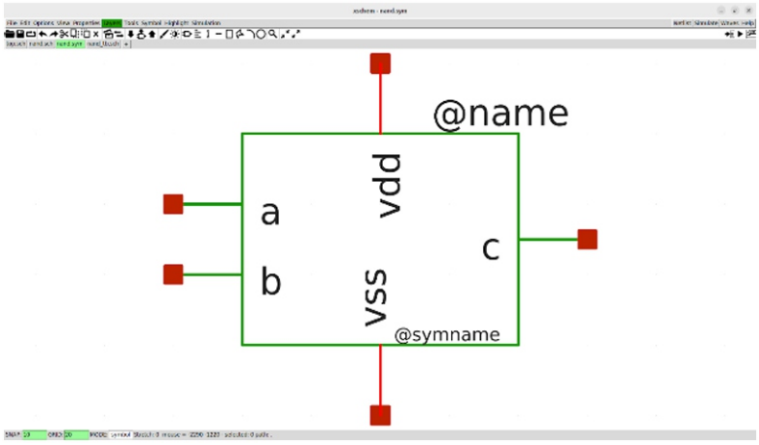


Fig. 1.3 NAND Gate Symbol

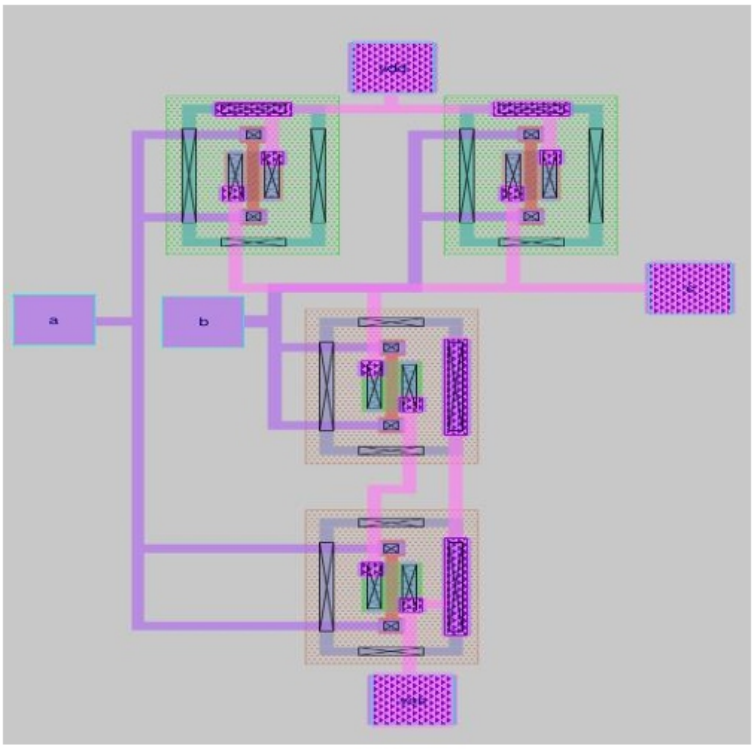


Fig. 1.4 NAND Gate Layout

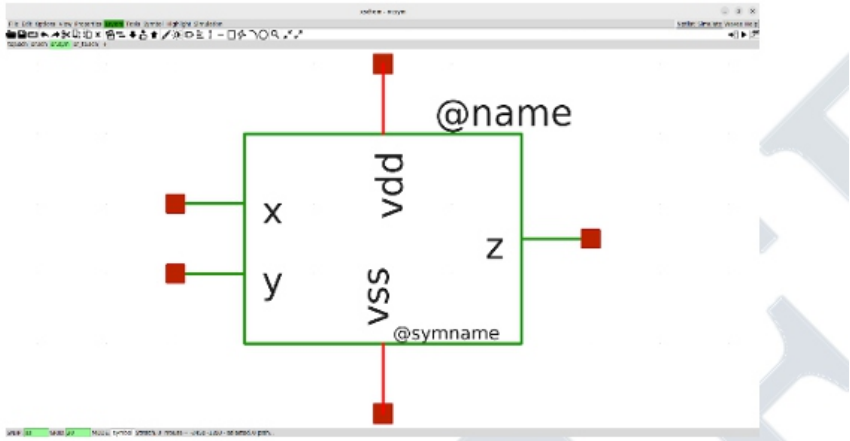


Fig. 1.5 OR gate Symbol

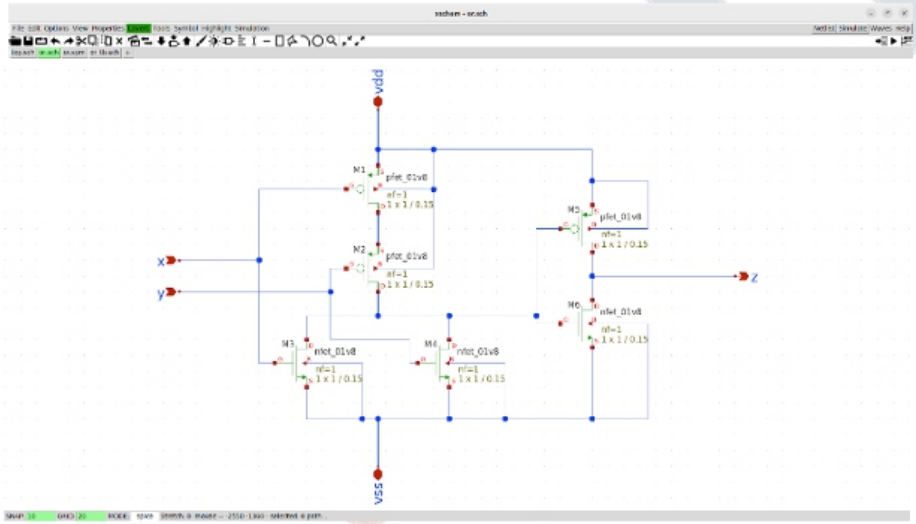


Fig. 1.6 OR gate Schematic

8-bit Adder from Full Adders:

In an 8-bit adder, the addition of two 8-bit binary numbers is carried out using a series of full adders. Each bit addition is handled by an individual full adder, with the least significant bit (LSB) to the most significant bit (MSB) being connected to the corresponding inputs of these adders. Each full adder's carry output is fed into the carry input of the next higher bit full adder. The sum output from each full adder represents the respective bit of the final sum. The total carry-out for the entire 8-bit addition is indicated by the carry output of the last complete adder. Thus, the 8-bit adder is structured with 8 full adders arranged in a cascade, where the inputs are tied to the specific bits of the numbers being added, and the outputs generate the 8-bit result.

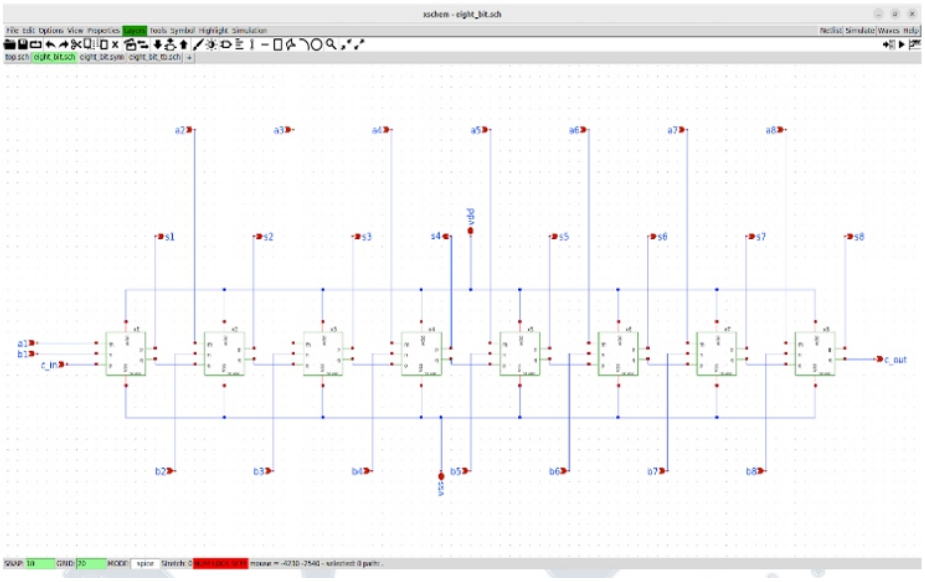


Fig: 1.7 8-bit adder schematic

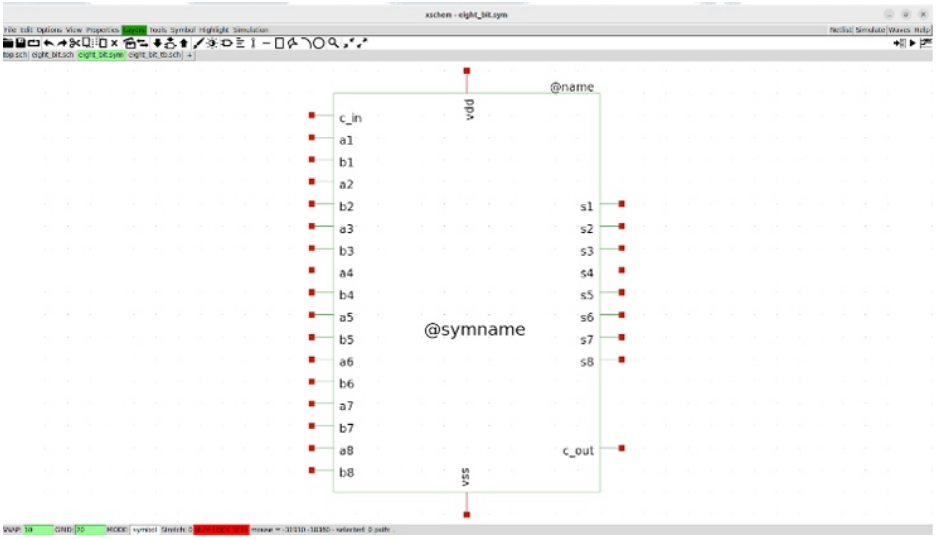


Fig. 1.8: 8-bit symbol

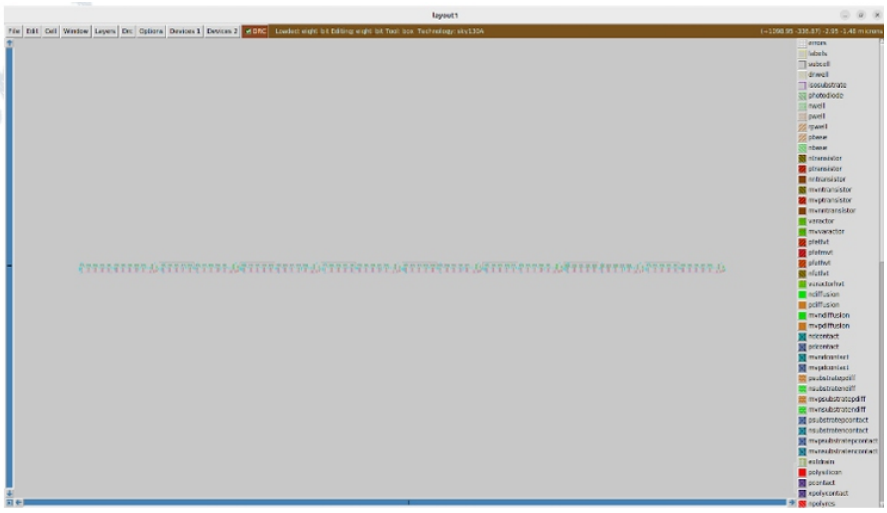


Fig. 1.9: 8-Bit layout

64-bit adder:

A 64-bit adder adds two 64-bit binary numbers together. Implement each segment of the 64-bit addition using an 8-bit full adder. Segment the 64-bit numbers into 8-bit chunks. Connect corresponding bits (from least significant bit to most significant bit) of both numbers to the inputs of the respective 8-bit full adders. Propagate the carry output (c_out) of each 8-bit full adder to the carry input (c_in) of the next higher significant bit's 8-bit full adder. Take the sum output from each 8-bit full adder as the corresponding bits of the output sum. The carry output (C_OUT) of the last 8-bit full adder represents the carry-out for the entire 64-bit addition. The 64-bit adder consists of 8 8-bit full adders connected in a cascade fashion with inputs connected to the respective bits of the input numbers and outputs forming the 64-bit sum.

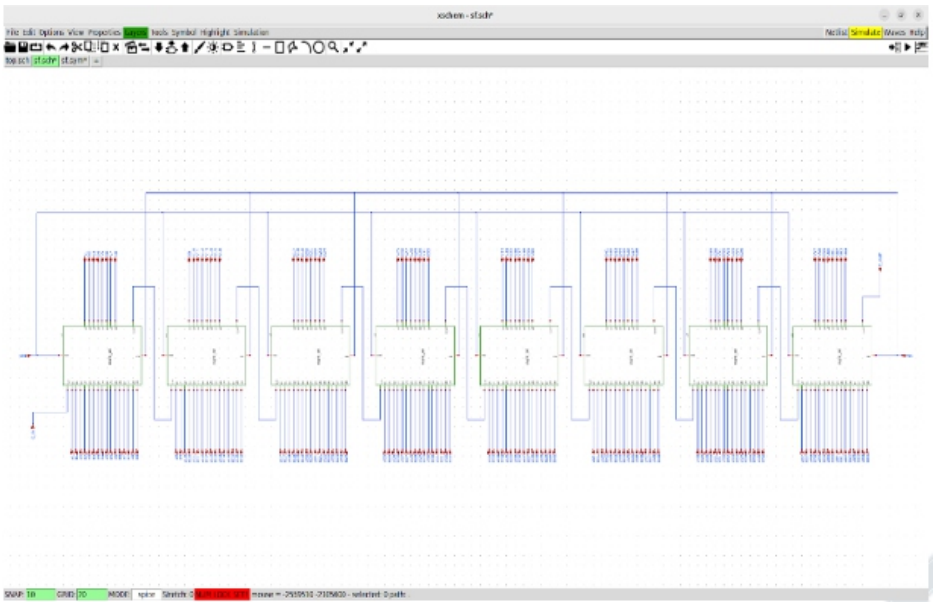


Fig.2.0: 64-bit adder schematic

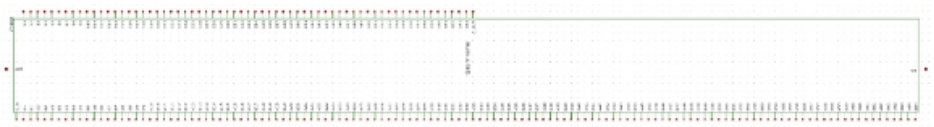


Fig.2.1: 64-bit adder symbol

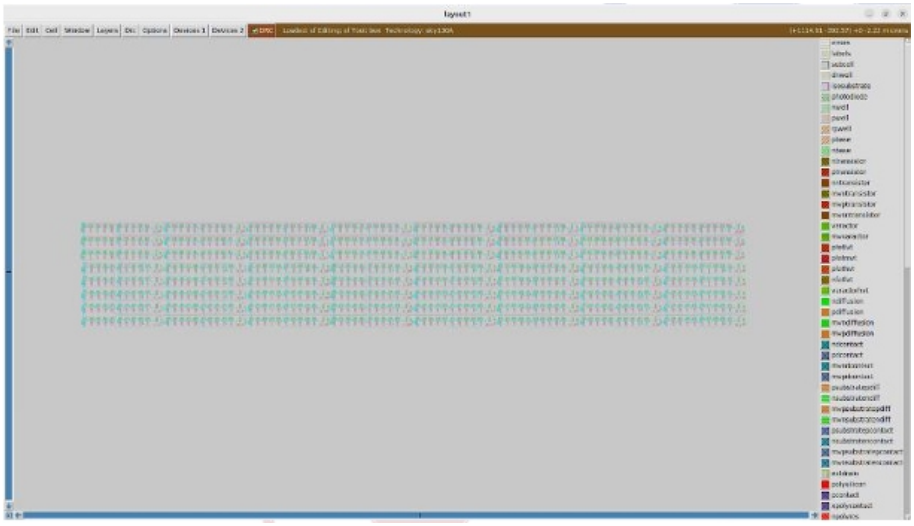


Fig.2.2: 64-bit adder layout

IV. RESULT ANALYSIS

Power analysis, simulation analysis, delay time analysis & area analysis are the major parameters to be focused in this section. The power analysis and delay time analysis were performed using the open-source tool NGSpice. The hierarchical design, netlist generation and schematic was designed using Xschem. To test further area analysis, SKY130 PDK was used. The detailed analytical procedure is as follows.

POWER ANALYSIS:

Power is being analyzed in netgen. Power is crucial to understand design's energy consumption. It is obtained by the formula:

Iavg*Vdd

ie. product of average current flowing from the Vdd branch and the supply voltage (1.8v) over one period of time. In result negative sign shows the absorption of power 1.66µw. Figure shows the output of netgen.

$$P = Iavg*Vdd$$
$$= -1.66\mu W$$

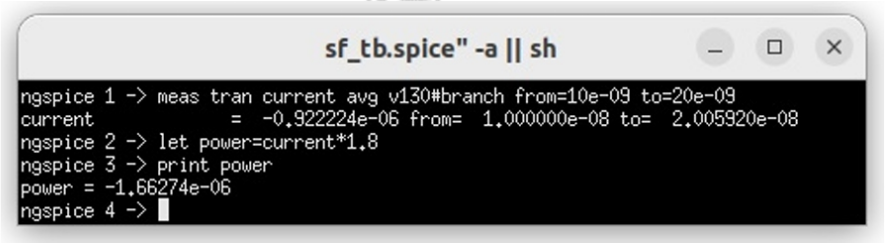


Fig.2.3 Power calculation

SIMULATION ANALYSIS:

To verify the functionality of these circuits, a test bench is generated for a half adder and full adder in Xschem by creating a simulation environment. This will help in validating their operation under the defined input conditions. The pictorial representation of simulation analysis is shown in Fig.2.4 and Fig.2.5.

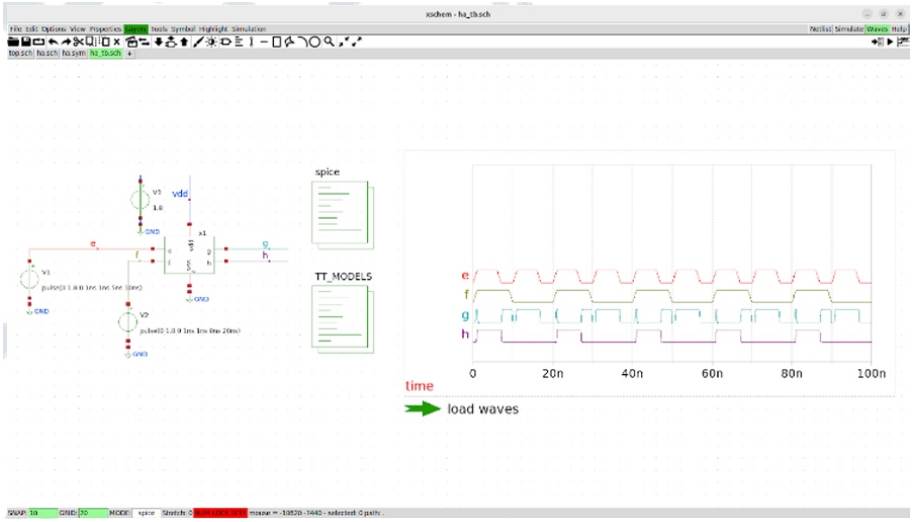


Fig.2.4 Half adder test bench

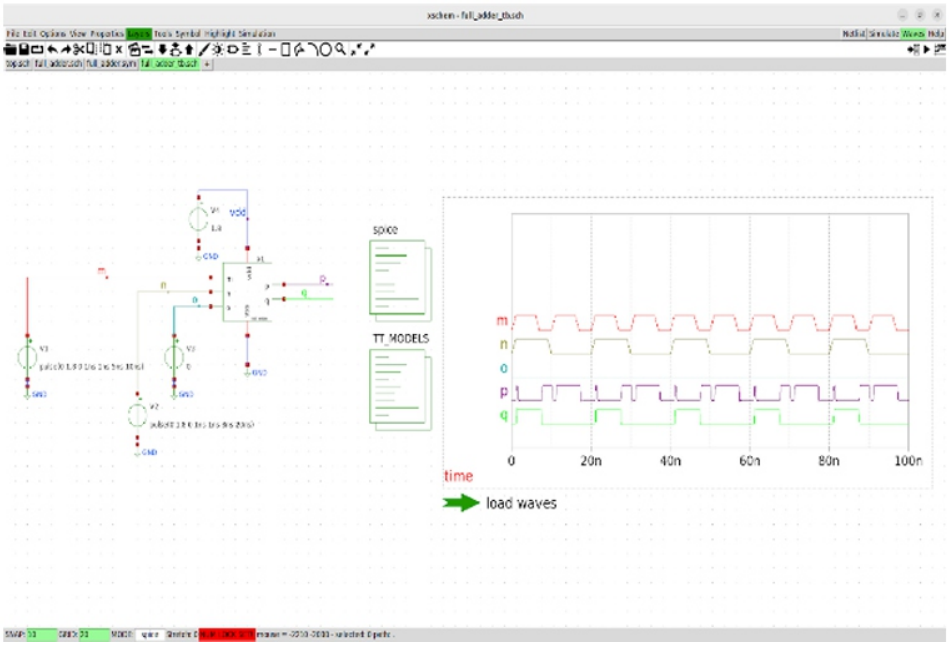


Fig.2.5 Full Adder Test Bench

III. DELAY TIME ANALYSIS:

Delay time analysis also known as propagation delay refers to evaluating the time taken for the adder to produce the correct output after receiving the input signals. It is obtained by taking the average of time taken by signal to travel high to low Tphl and time taken by signal to travel low to high level Tplh. It is obtained by the formula:

$$\mathbf{Tp = (Tphl+Tplh)/2.}$$

The pictorial representation of delay time analysis is shown in the Fig. Secondly Fig. shows the calculation of delay time analysis of 2.545ns.

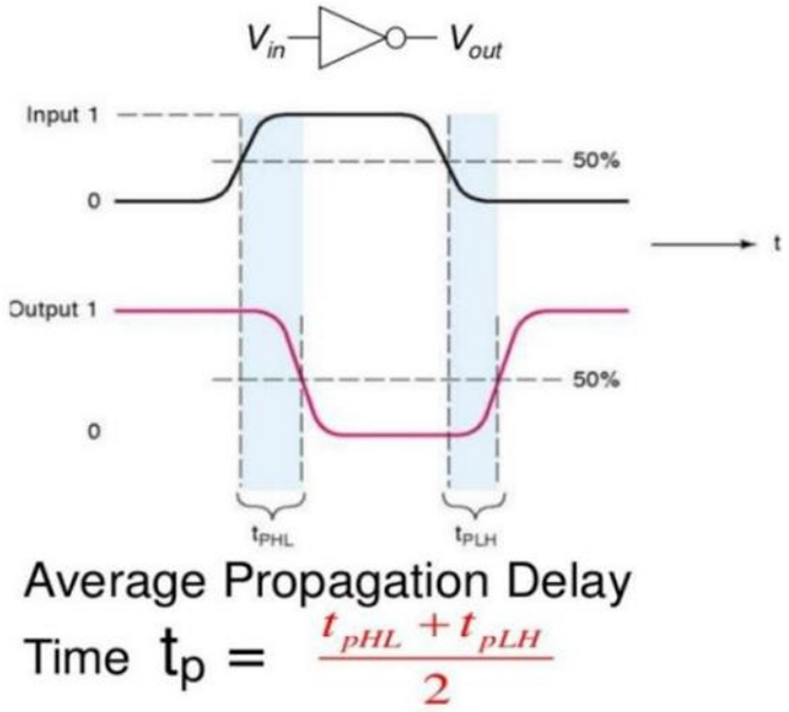


Fig.2.6 Delay time Analysis

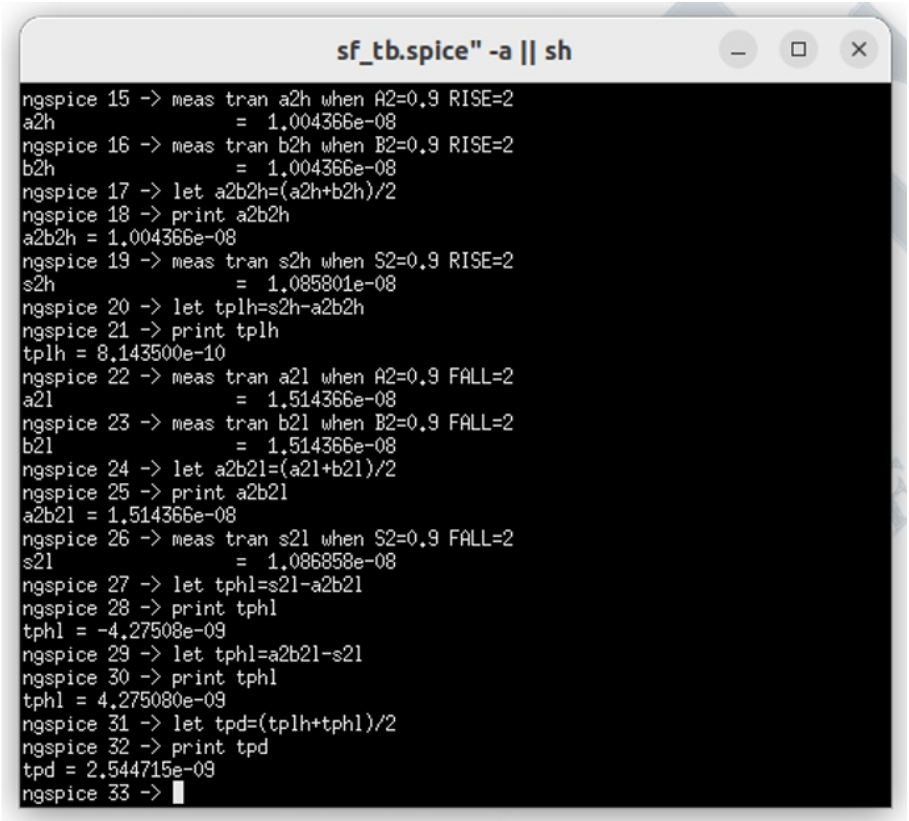


Fig.2.7 Delay calculation of 64-bit full adder

IV. AREA ANALYSIS:

Area analysis of a layout refers to evaluating the physical size or footprint occupied by the circuit design on the semiconductor chip. For a 64-bit adder layout, area analysis provides insights into the layout's size, which is a critical factor influencing chip area utilization, manufacturing cost and overall integration density. Area analysis is being performed by integrating open-source tools Magic VLSI and SKY 130 PDK. At last after verification and design rule check (DRC), area analysis is obtained to be 168170.859 sq nm. The following fig displays the area analysis.

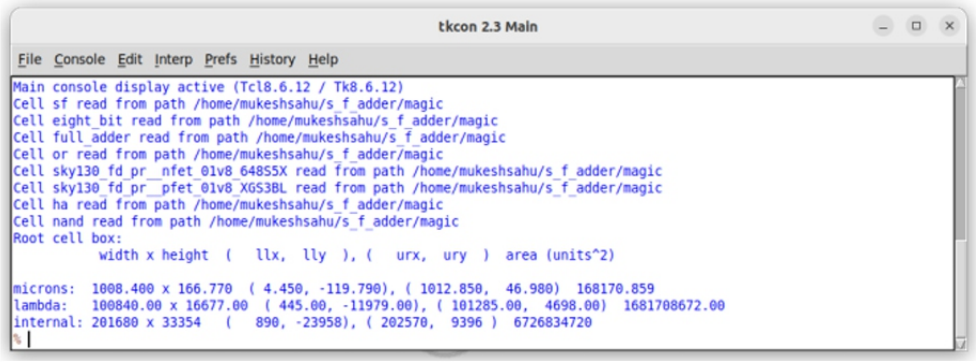


Fig.2.8 Area Calculation of 64-bit Full Adder

Table I. Performance analysis at different technologies of 64-bit Full Adder

Technology(nm)	Power consumption(µw)	Time delay(ns)
180-nm	4.15	0.22
130-nm (Proposed design)	1.66	2.54

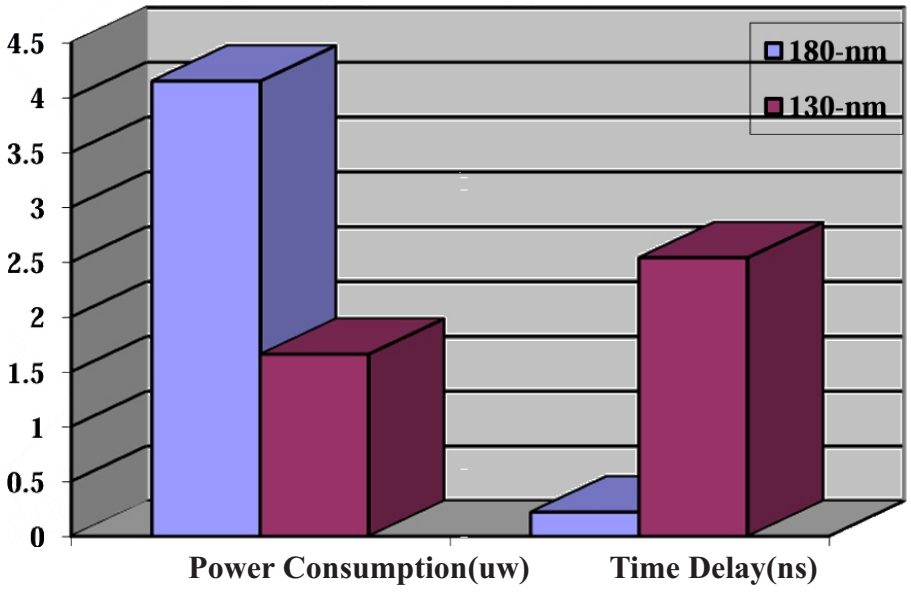


Fig.2.9 Power and delay comparison

V. CONCLUSION

A comprehensive design and execution of 64-bit full adder is tested and proposed in this paper. This research successfully demonstrates the design and implementation of a 64-bit full adder using the Sky130 process technology, leveraging the open-source tools Magic VLSI and Netgen. This research underscored the importance of meticulous design, verification processes like Design Rule Checking (DRC) and Layout vs. Schematic (LVS), and simulation to ensure circuit functionality and compliance with design rules. By minimizing the most of logical components of the design structure, it will be helpful to decrease area and power consumption. The author claims that the proposed 64-bit full adder at 130nm technology has a power consumption of 1.66µWalong with propagation delay of 2.54ns at area efficiency of 168170.859 sq nm. This work not only underscores the viability of the SkyWater 130 nm technology for advanced digital circuits but also paves the way for future innovations in the domain of low-power, high-speed arithmetic units. On the basis of this foundation, future studies can investigate additional improvements and applications in more intricate computational systems. From the given proposed design of 64bit full adder, in future 128bit full adder can also be design.

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A B S T R A C T

Robotic grippers have become an emerging trend due to their boundless applications in industrial automation. A gripper is a mechanism that allows you to manipulate the holding of an object. A gripper can grab, tighten, handle, and release an object. Deploying unmanned aerial vehicles, especially Hexacopter for last-mile delivery is the aim of this project. The Proposed work has the ability to autonomously carry a payload minimum of 10 kg. In this project, a robotic gripper with the ability to grab objects is attached to the drone to carry the load autonomously. With the increasing capabilities of robotic systems, their applications have been promoted from industrial areas with simple and repetitive tasks to more unknown areas with more complicated applications. The robotic gripper arm is controlled by the Digital servo motors which are used to grab the load. The gripper is configured using the Arduino boards. The hardware part of Arduino comprises Arduino boards, input and output devices (including digital and analog pins, and sensor actuators), shields, breadboards, jumper wires, and so on. The software consists of the development tools needed to write, debug, compile, and upload code to Arduino boards. Most of the software tools are available in the Arduino IDE (Integrated Development Environment). Arduino boards are programmed in C.

Index Terms—Arduino, Hexacopter, Robotic Gripper

I. INTRODUCTION

Multi-rotor aircraft are typically small unmanned aerial vehicles (UAVs) used for aerial photography, Traffic Monitoring, Aerial Measurements, Fire Detection, Monitoring, and Extinguishing, [13] surveillance, and recreational flying. Multi-rotor aircraft are popular due to their simplicity, agility, and ease of control. Dynamic aerial grasping [1] is a recent research challenge that bears much potential to enable many new applications in automation and hard to reach places. Multi-copters and soft robotic grippers are a natural match for aerial manipulation as they are easy to maneuver and provide much versatility as a research platform. These properties have been beneficial for multicopter in a wide range of applications such as point-to-point deliveries [2] and aerial manipulation [3].While there is extensive previous work on normal flights, recent approaches continue to incorporate new features of Rotorcraft platforms [4],[5],[6]. The arm-like structure of an industrial robot is known as a robot manipulator. An end-of-arm tooling (EOAT) device is an attachment that enables a robotic arm to manipulate things.

End of arm tooling devices, like grippers allows the drone used in machine automation to manipulate and move an object. Mechanical grippers can be either twofingered or three-fingered, depending on the gripping requirements.Mechanical grippers find applications in industries such as automotive manufacturing, where they are used for material handling , pick and place operations.

II. RELATED WORK

Combining robotic grippers with flying platforms opens a new dimension for aerial object transfer. Hiranmayee Panchangam[10] developed a mini controller arm which picks and places things as desired,the control the Robotic arm not only by using the wired controls, but with the aid of the Internet of Things which introduces automation in the system. J. Fishman, S. Ubellacker, N. Hughes, and L. Carlone [1] creates soft drone - a quadrotor where traditional landing gears are replaced with a soft tendon-actuated gripper to enable aggressive grasping.Tae-Yoon Kim and Jae-Hyun Kim [4] designed an unmanned aerial system (UAS) in a surveillance environment that includes a relay system.System provides the drone communication from Ground Control Station(GCS) to the long-distance areas that want to observe through wireless communication enhancement in dangerous situations. Surveillance drone records video, and it is used to find specific people in dangerous areas. Viral Kumar Goyal , Abhishek Kamal , Adarsh , Pratapbhan Singh , Vernika Singh [6] Quadcopter of plastic fame and polycarbonate propellers with “TS832 transmitter” used to transmit and “RC832S receiver” to receive signal from the Remote Controller. An arduino module is attached to the digicam which sends the data in the form of video and images to the control center. Haar cascade classifier to detect human face and LBPH algorithm that recognize human. Ron Oommen Thomas and Prof. K. Rajasekaran [11] designed a robotic arm controlled by using the raspberry pi module .It monitors the movements and actions of robotic arm.

III. PROPOSED WORK

This project aims at introducing a multi-rotor that can fly to the accident spot with the required medical aid like Automated External Defibrillator (AED), Cardio Pulmonary Resuscitation (CPR) and can be used to transport blood products ,mini oxygen cylinders and even human organs. The main purpose of this project is to develop a drone which can carry the load from one place and drop it in the another place. This project uses a 6-motor drone which is called Hexacopter which increases the stability during the flight and also increases the load-carrying capacity. The Drone lifts the carrier box using the gripper which is attached to the base of the Hexacopter. The Tower Pro MG995 Servo Motors, each attached to a mechanical arm metal claw are the foundation of the Gripper's design. A gripper module, which consists of four arms each driven by a high-speed servomotor. An Arduino Nano microcontroller controls each of the four arms of the gripper module, which is fastened to the drone's underside. The drone's flight controller and Arduino are connected. The Mission Planner software used in this project controls the drone's location and allows it to function autonomously.The Drone returns to its original location using the one-touch return mechanism once the task is completed.

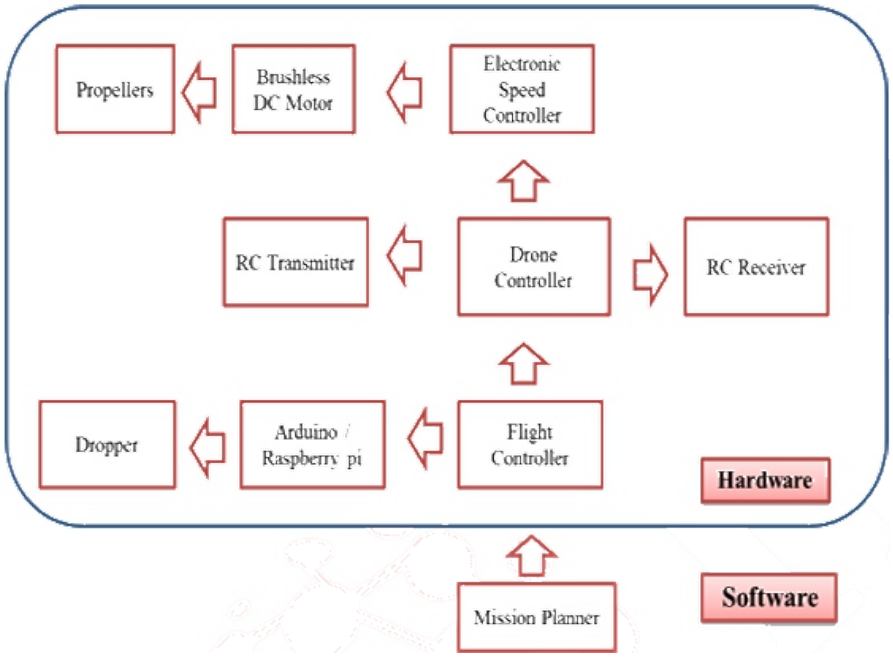

Fig 1: Block Diagram of the Proposed system

IV. SYSTEM ARCHITECTURE

A. System Components

For structures just like the drone, there exist already off the shelf components that allow us to compose our systems reducing the need for specialized development. This permits us to focus on creating a strong gripping system. Our system consists of three subsystems: the drone, the gripper module, offboard components, and Middlewares.

1) Drone Body:

Hexacopters are very similar to the quadcopters, but they provide more lifting capacity with the extra motors. The hexacopter [12] has 6 motors mounted typically 60 degree apart on a symmetric frame, with three sets of CW and CCW motors/propellers. We placed the different components to provide easy access to the various functional units. We modified the EFT E610 platform to achieve our objective of a lightweight design .The drone's body is comprised of industrial materials such as cardon fibre, making it extremely sturdy and smooth.The foldable propellers make it simple to transport.

transport.

- To keep the weight of the drone as low as possible EFT E610 carbon fiber frame is used
- Carbon fiber is used in the drone's structure or frame because of its high strength and light weight.
- **Frame weight** - 5 kg approx
- **Wheel base** - 1404mm
- **Arm diameter** – 30 mm (6 axis)
- **Opening size** - 1495 X 1308 X 500mm
- **Folding size** - 945 X 848 X 500mm
- **Landing Gear** – 304 mm height
- **Supports take off weight** – 35 kg

2) Motor and Propeller :
Weight of drone = Mass (Frame weight + batteries +
Equipment weight) x gravity
Weight = 35(approx) x 9.81
Total thrust= 343.35 N or 35 kgf
(1kgf = 9.8 N)
Since we are using hexacopter i.e 6 propellers
Thrust per motor = Total Thrust/number of motors
Thrust per motor= 35 / 6
Each propeller Thrust = 11.667 kg

Here we use Hobbywing XRotor X6 Plus Motor with the following specification:
• Motor KV Rating -180 kV
• Have inbuilt ESC – No ESC needed
• Fibre Tube Propeller -2480
• Max Thrust: 11.8 kg
• Recommended Weight - 3-5 kg
• Battery – 12 S

Fig 2: Hobbywing XRotor X6 Plus Motor

To determine the propeller size we have to follow certain parameters:
• Drone frame size determines the diameter of the propeller
• Calculate the straight line distance between 2 adjacent axes and the angle between them, the distance is the max of the propeller • To find the distance between the axes, we use cosine formula,

$$c^2 = a^2 + b^2 - 2ab\cos(\gamma)$$

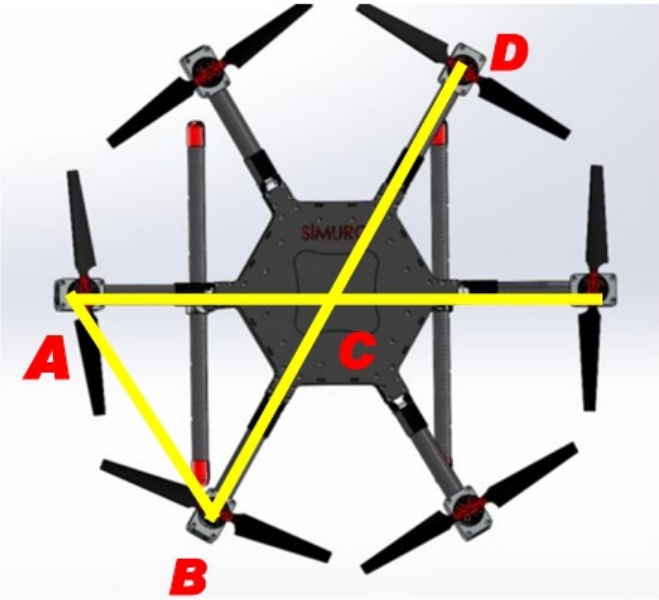

Fig 3: Angle of Hexacopter Frame

We used the frame of Wheelbase - 862mm
$AB^2=AC^2+BC^2-2AC \cdot BC \cdot COS(\beta)$
$=431^2+431^2-2(431)(431)(COS\ 0)$
$=185761+185761-2(431)(431)(0)$
$AB^2=371522mm$
1 inch = 25.4mm
AB =609.53/25.4
AB =23.99 ~ 24 inch
Hence we use 23-24 inch propeller.

3) Flight Controller

The flight controller is the brain of the hexacopter drone, responsible for interpreting pilot inputs and sensor data to maintain stability and control during flight. It utilizes various sensors, Several flight controller options are available in the market,we choose Jiyi K++ Version 2 Flight Controller. Electronic Speed Controller is an electronic circuit which is used to change the speed and direction of brushless motor. Basically, an ESC converts DC battery power into 3-phase AC for driving Hobbywing X6 BLDC Motors. Here we use Hobbywing Skywalker- 80A UBEC which comes with the BEC, battery eliminator circuit, which delivers the electric power to other circuitry without the need for multiple batteries.

Specification of the Flight controller

• Supported frame types:
Quadcopter (+, X)
Hexacopter (+, X, IY and YI coaxial twins)
Octocopter (+ type, X type, V type)
• Supports ESC control: up to 1000Hz
• Supported receiver types: PPM, S-BUS receiver

• Supported ESC type: 490HZ or less PWM ESC
• Power consumption: less than 5W
• SBUS receiver Maximum vertical speed: 6 m / s
• Hardware specification
The Jiyi K ++ V2 flight controller comes with two Power Management Unit (PMU's), GPS,FC,LED. Jiyi K ++ V2 flight controller is configured by the Jiyi K ++ V2 flight controller software

Fig 4: Jiyi K ++ V2 flight controller

4) Remote Controller
Drone controllers serve as the primary interface between the pilot and the drone, allowing for seamless control over its flight and movements. They consist of a transmitter, responsible for sending signals to the drone, and a receiver, which receives signals from the drone. Communicating through radio frequencies, typically in the 2.4 GHz range, drone controllers enable pilots to command their drones with precision and accuracy.A drone transmitter uses many frequencies like 27MHz, 72MHz – older frequencies ,433Mhz, 900Mhz, and 1.3GHz – long range FPV and RC system ,2.4Ghz – Provides Frequency Hoping . Most transmitters work on 2.4GHz for accuracy.
The range of a drone's controller depends on factors such as frequency, power, and interference.
We can determine the range of a RF by using the equation,

$$R = (10^{(Pt + Gt + Gr - Pr - Lf + 60)/20}) / 41.88 * F$$

Where,
Pt = Transmission Power
Gt = Transmitting Antenna Gain
Gr = Receiver Antenna Gain
Pr = Receiver Sensitivity
Lf = Loss factor
F = frequency of the signal

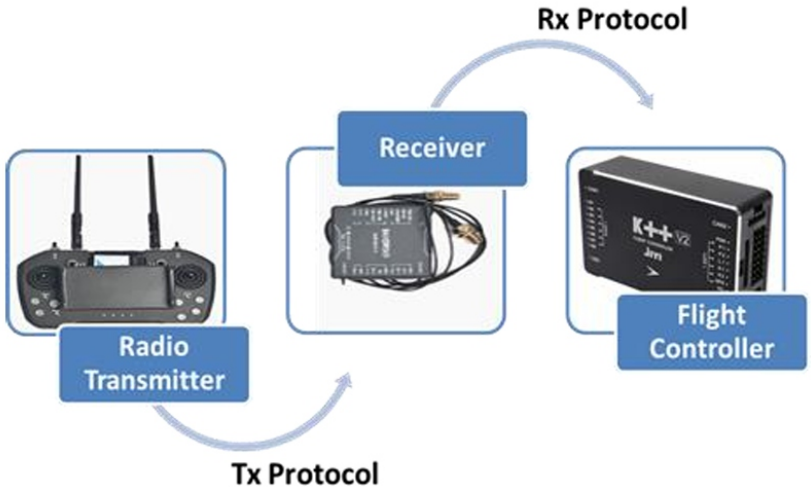

Fig 5: Tx & Rx Protocol

Here we use Skydroid T12 Remote Controller with specification:

- **Frequency:** 2.400-2.4833GHz
- **Duration:** 25 hours
- Uses the latest FHSS technology (Frequency hopping Spread Spectrum)
- up to **20 KM** transmission

Fig 6: Skydroid T12 Remote Controller

5) Gripper Architecture

An end-of-arm tooling (EOAT) device is an attachment that enables a robotic arm to manipulate things. EOAT provides a "hand" that can perform a variety of functions. There are numerous end-of-arm tooling devices available.One of the most prevalent kinds of end of arm tooling is the gripper, which can grasp and release parts in an automation project. Most grippers or pick-and-place units have precise mounting surfaces for specific attachments. The Gripper is designed with four Tower Pro MG995 Servo Motor

each connected with Mechanical Arm Metal Claws. The Gripper arm's Claw is made up of aluminum alloy material with the Degree of Freedom (DOF) two. The Servo motors are used to perform "twist" and "grasp" movements to manipulate objects with the gripper. The Arduino is used to to optimize robotic control. The servos can control the gripper to open upto 55mm from closed state.

Determining the griping force and torque required to Pick

an object
Grip Force = Part Weight x (1+Part Gs) x Jaw Style factor
Grip Force Required = 10 kg x 3 x 1 = 30 kg
Jaw Torque = Jaw Length x Grip Force
Jaw Torque = 4" x 30 pounds = 120 kg
Part Torque= Jaw Length x Part weight x Acceleration
Part Torque = 4" x 10 kg x 2 = 80 kg
Total Torque = Jaw Torque + Part Torque
Total Torque: 120 kg + 80 = 200 kg
Specifications: 10 kg of grip force, 200 kg of torque

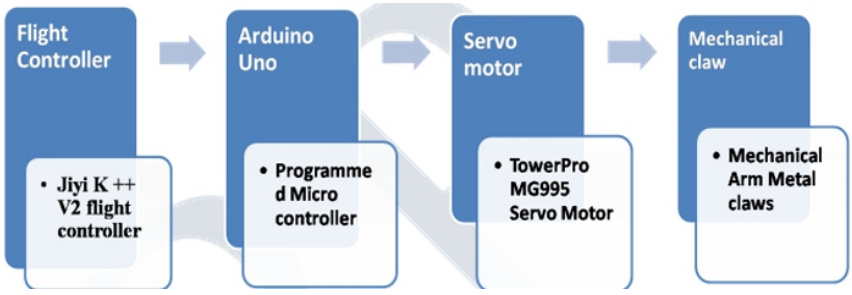

Fig: 7 Flow diagram of Gripper model

B. Software Components

1) Flight Control Software
Jiyi K ++ V2 flight control software includes four functional interfaces:
• Viewing,
• Basic,
• Advanced and
• Tools

2) ARDUINO UNO
The Arduino Web Editor is a web-based integrated development environment that includes online storage. The Arduino IDE, as it is often known, is an integrated development environment. To program your board, first write a program, then compile it into machine code, and finally deliver the new program to your board. The Arduino IDE makes all of this possible, from the first line of code written to its execution on the Arduino board's microcontroller. It is a program or application that may be downloaded (or used online) to manage your entire code development process.
There are three Arduino IDEs available:

• Arduino IDE 1.8.x (classic)
• Arduino IDE 2 (new)
• Arduino Web Editor (online)

V. EXPERIMENTAL RESULTS

Experiment is carried on with the model to check the loading capacity of the model. The model is subjected to carry the load of different weights. Below Table shows the success rates to pick up the object for the 15 attempts for weights 1kg, 2kg, 5kg, 7kg and 10kg.The object of each weights is picked from one location and dropped at the distance of 5 meter apart. Both manual and automatic dropping system is tested. One-touch return mechanism is also tested.

Objects/ Weights	No. of Trails	No. of Successful Attempts	Success Rate (Percent)
1 KG	15	15	100
2 KG	115	15	100
5 KG	15	14	93
7 KG	15	14	93
10 KG	15	13	86.66

VI. RESULT AND CONCLUSION

This research presented the design and development of a robotic gripper for a Hexacopter drone, facilitating autonomous last-mile delivery. The proposed system offers a minimum payload capacity of 10 kg, making it suitable for a wide range of delivery needs. Future work can explore advanced gripper designs, integration with object recognition systems, and enhancing the gripper's autonomy for secure and efficient package delivery.

Fig 8: Proposed Model

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A Portable, Image-Based Iot Detection System for Real-Time Traffic Signs, and Vehicles

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ABSTRACT

With the rapid advancements in computer vision and deep learning technologies, the integration of IoT (Internet of Things) has ushered in a new era for enhancing driving safety and reducing traffic accidents. While modern cars typically come equipped with integrated ADAS systems, there's a gap for vehicles lacking such built-in capabilities. This paper proposes a portable, image-based IoT system tailored for real-time detection of crucial elements such as traffic signs, vehicles, and pedestrians. To achieve seamless real-time detection, our system harnesses the power of the YOLO v8 algorithm. This algorithmic framework enables efficient processing of visual data, ensuring swift and accurate identification of pertinent objects on the road. By leveraging Io T, our system transcends the limitations of traditional ADAS setups, offering a flexible solution that can be easily deployed across diverse vehicle types. This single-stage detector is very popular as it has high detection speed and accuracy. This approach utilizes ultrasonic sound sensor technology to detect and convey messages to the driver regarding nearby vehicles approaching their car. It assesses the proximity between two vehicles traveling in the identical lane and direction, providing real-time feedback to the driver. Through the combination of IoT and advanced computer vision algorithms, our portable system empowers vehicles of varying makes and models with intelligent detection capabilities.

Keywords— Accident detection, Collision Avoidance, Ultrasonic sensor, YOLO v8 Algorithm, GSM module, GPS, Vibration sensor.

I. INTRODUCTION

In recent years, the advancement of automobile technologies has unfortunately paralleled a surge in road accidents, resulting in devastating loss of lives and significant societal impact. One critical challenge exacerbated by such incidents is the delay in emergency response, particularly during the pivotal "golden hour," wherein swift medical intervention can significantly improve survival rates. Recognizing the urgency to address this pressing issue, innovative approaches integrating cutting- edge technologies have emerged to enhance road safety and expedite emergency response mechanisms. Among these advancements, the use of machine learning algorithms for predictive analytics stands out, empowering systems to anticipate potential hazards and adapt driving behaviour proactively based on historical data insights encompassing traffic patterns, road conditions, and driver behaviour [11].

Moreover, advanced communication capabilities play a pivotal role in fostering seamless interaction among vehicles and infrastructure, facilitating real-time exchange of critical information regarding road conditions, traffic congestion, and emerging hazards [13]. Leveraging vehicle-to-vehicle (V2V) and vehicle-to-infrastructure (V2I) communication protocols, these systems enable collaborative decision-making and coordinated responses to mitigate potential risks effectively. Additionally, prioritizing user experience and accessibility, these systems incorporate intuitive interfaces and user- friendly controls, ensuring drivers can easily comprehend and interact with safety features for enhanced usability and adoption.

Furthermore, recent advancements have seen the integration of IoT-based technologies to prevent accidents by monitoring both external and internal driving conditions comprehensively. This entails the monitoring of road conditions and alerting drivers to hazards externally, while internally focusing on factors such as oxygen levels and driver fatigue [11]. The study suggests using clustering with Road Side Units (RSUs) monitored by Artificial Intelligence (AI) to cut down accidents in India. Vehicular Ad hoc networks (VANETs) aid communication between vehicles and infrastructure, sharing warnings about road conditions and traffic violations. AI-driven data transmission enhances Quality of Service (QoS), improving Packet Delivery Ratio (PDR) and throughput values [12]. Forecasting road accidents in the DVRE system involves statistical analysis to assess factors' impact and evaluate safety measures. Visual methods identify conflict situations, while potential danger methods predict accident risks. An integrated approach combines prediction methods with on-site inspections, enhancing traffic safety assessment and forecasting accuracy [13]. Variable speed limit (VSL) is an intelligent transportation system (ITS) solution for traffic management. The speed limits can be changed dynamically to adapt to traffic conditions such as visibility and traffic volume, curvature, and grip coefficient of the road surface. The VSL traffic sign location problem and attempts to solve it using computer simulation are presented in this paper. Experiments on a selected road segment, carried out using the traffic simulator, have shown that the proposed method allows the driver’s habits to be taken into account so that the location of road signs can be optimized. The observable effect was a reduction in vehicle speeds and speed variance on critical road segments, translating directly into increased safety and harmonized traffic [33]. Smart features like adaptive speed reduction and intelligent bump detection further augment driving safety, while real-time data processing and analytics enhance overall system efficiency and effectiveness.

As we delve deeper into these advancements, it becomes evident that a holistic approach to driving safety is imperative, encompassing real-time detection, proactive risk mitigation, intelligent communication, and user-centric design principles. By combining these elements seamlessly, these systems aim to redefine the standards for intelligent driving systems, setting new benchmarks for safety, efficiency, and user experience in the automotive industry. Consequently, these innovative solutions hold the promise of significantly reducing accident rates and human casualties, ushering forth a new epoch of road safety and security.

II. RELATEDWORKS

To prevent car accidents by monitoring both external and internal driving conditions. The external part monitors road conditions and alerts the driver to hazards, while the internal part focuses on factors like oxygen levels and driver fatigue.Smart features like adaptive speed reduction and smart bumps are suggested for safer driving. By connecting sensors and actuators, the system aims to mitigate accident

risks effectively [11]. The rise in vehicles has led to crowded roads and increased road accidents, with fatalities rising by 31% from 2007 to 2017 in India. Vehicular Ad hoc networks (VANETs) aid in accident prevention by facilitating communication between vehicles and infrastructure, sharing warning messages about road conditions and traffic violations. Despite efforts like speed limits and safety features, accidents persist. This study proposes a clustering approach with Road Side Units (RSUs) monitoring using Artificial Intelligence (AI) to reduce accidents in India, leveraging VANETs for communication and traffic control. The hybridization of AI techniques accelerates data transmission, with improved Quality of Service (QoS) parameters, as shown by increased Packet Delivery Ratio (PDR) and throughput values [12]. Methods for forecasting road accidents in the Driver–Vehicle–Road–Environment (DVRE) system include statistical analysis to evaluate the influence of different factors and evaluate road safety measures. Visual methods identify conflict situations to understand subsystem interactions, while potential danger methods predict accident risks and fatalities. Evaluating changes in accident rates post-safety measures is vital. An integrated approach combines accident prediction methods with on-site inspections, including black spots evaluation, to enhance traffic safety assessment and accident forecasting accuracy [13].

III. METHODOLOGY

This section outlines the system's architecture and the dataset employed for this study. Furthermore, it provides a comprehensive overview of the model's training and testing procedures.

A. Overview of the Proposed Architecture

This work follows the diagram in Figure 1 for real-time detection and recognition of traffic signs and road objects. The presented diagram for this work is based on a YOLO v8 model. The dataset was organized by preprocessing the data. Using the YOLO v8 architecture, classes for development of the TSDR systems were trained with this dataset, and a trained model file is obtained with 80% training of our model and 20% in the testing process. This model was evaluated to measure the implementation metrics of training and testing performance in realtime.

B. Data sets

The datasets of work includes the various speed limits of 30KM, 60 KM and 80 KM and also speed breaker and school Zone.The images are collected in various places.

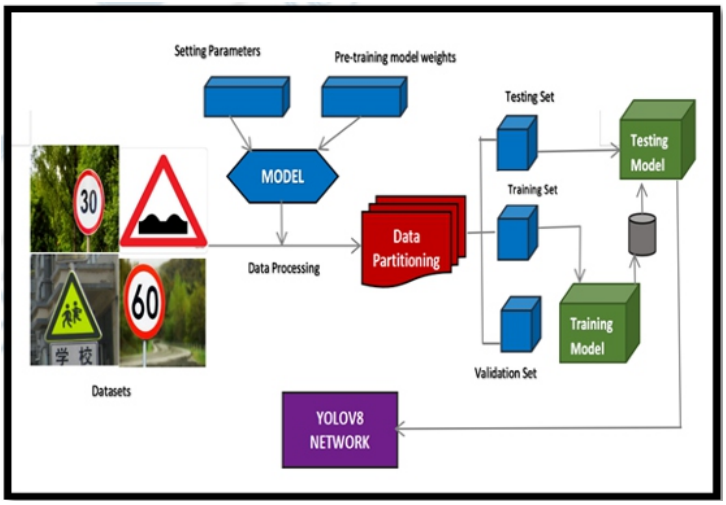

Fig. 1. Proposed Methodology of YOLO V8

C. Training Stage

In order to obtain a robust system that works stably under different illumination and environmental conditions, the model must be trained with an appropriate dataset. At this stage, it is very important to determine in what proportion the dataset should be divided. In this work, data labeled for training in the dataset is divided between 80% and 20% for training and testing. The proposed system can detects vehicles, pedestrians, and traffic signs accurately and quickly with a cam- era in real-time. Deep learning applications require high computational power and processing speed due to too many hidden layers, constant weights updating, and increasing training parameters. To successfully perform the recognition operations, the model must be well trained.

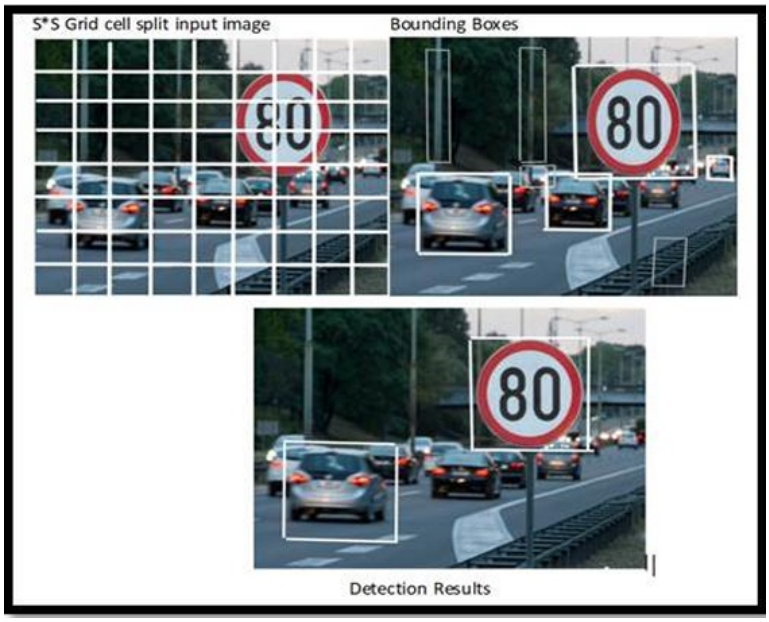

Fig. 2. Conceptual Design of YOLO Algorithm

D. Detection Model Selection

Object detection is the process of recognition and locating objects in images. Many architectures and models have been proposed in terms of accuracy and speed in the literature. This work used the YOLO v8 network to developed model. Backbone Architecture: YOLOv8 might incorporate advanced backbone architecture for feature extraction. This could involve a highly optimized backbone network, possibly based on recent advancements in convolutional neural networks (CNNs) such as EfficientNet or ResNeXt. The backbone network plays a crucial role in capturing meaningful features from input images.

E. Yolo Network Architecture

YOLO is a fast, high-performance real-time algorithm that uses CNN to better detect objects. Unlike previous algorithms, it performs the detection process with a regression- based approach [26]. Traditional object detection models, such as RCNN, offer an area of interest (RoI) for convolution [31], [32], while YOLO does detection and categorization at one time. YOLO achieved this process by passing the input photograph through a single CNN network. In YOLO, the input image undergoes segmentation into regions, where bounding boxes and class probabilities are estimated individually for each region. Its conceptual design repeats the process in real-time for each image input as depicted in Figure 2. The algorithm's network model aims to detect cells tasked with detecting the object.

F. Yolo V8 Based Detection and Recognition

Feature Fusion: YOLOv8 could employ sophisticated feature fusion techniques to integrate multi-scale features effectively. This could enhance the model's ability to detect objects at different sizes and aspect ratios. Feature fusion mechanisms like Feature Pyramid Networks (FPN) or Cross Stage Partial Networks (CSPNet) may be utilized for this purpose.

Neck Structure: Similar to YOLOv5, YOLOv8 might incorporate a "neck" structure for feature aggregation. This could involve the use of PANet or other attention mechanisms to refine and combine features from various scales or resolutions.

Head Architecture: The leading section of the network would be responsible for producing object predictions. YOLOv8 may employ a revised edition of the YOLO head, potentially with improvements in anchor box generation, prediction quality, or post-processing techniques.

Training Environment: YOLOv8 would likely leverage modern deep learning frameworks such as PyTorch or TensorFlow for model development and training. It may also utilize distributed training techniques and hardware accelerators to expedite the training process.

Model Optimization: YOLOv8 could focus on model optimization strategies to reduce the model size and inference latency while maintaining or improving detection accuracy.

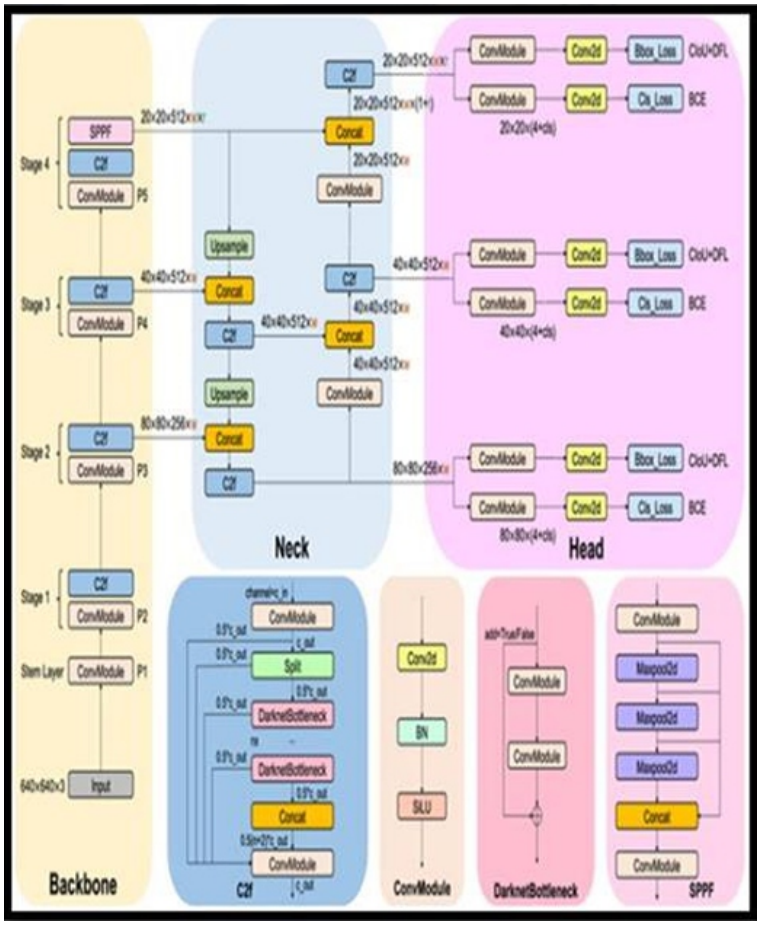

Fig. 3. Network Architecture of YOLO Algorithm

This may include methods such as model quantization, pruning, or knowledge distillation.

Performance Evaluation: YOLOv8 would undergo rigorous evaluation on benchmark datasets to assess its detection accuracy, speed, and efficiency compared to previous versions and other state-of-the-art object detection models.

Table I. Study of Various Literature Reviews

References	*Analysis Type*	*Application*	*Models*	*Techniques*	*Datasets*
Qian etal.2015 [2]	Video frames	Traffic Sign Detection	Based on multi task CNN	Region proposal, edge detection and CCA analysis	GTSRB, MNIST, CASIA GBI
Li et al.2015 [3]	Video frames	Traffic Sign Detection	Color segmentation, Shape symmetry based	Pyramid Histogram of Oriented Gradients(PHOG)	Study specific dataset
Yin etal.2015 [4]	Video frames	Traffic Sign Recognition	Feature based rotation, Invariant binary pattern	Hough-SIFT transforms Artificial Neural Network(ANN)	GTSRB and STS
Changzhen et al.2016 [5]	Video frames	Traffic Sign Detection	Based on Faster-R CNN	Region proposal Network(RPN)	Study specific dataset
Xu et al.2019 [7]	Video frames	Traffic Sign Detection	Based on adaptive thresholding, Shape symmetry	Cumulative Distributive Function, Shape symmetry detection	GTSRB dataset
Balado et al.2020 [8]	Images	Traffic Sign Detection and recognition	Based on Retina net and inception v3	Mobile mapping systems, point clouds, data fusion	GTSRB dataset
Jin et al.2015 [9]	Real-time	Traffic Sign Detection and recognition	Based on multi feature	Feature fusion and enhancement techniques	GTSRB dataset
Wan et al.2021 [10]	Images	Traffic Sign Detection and recognition	Single Shot Detector(SSD)	Improved YOLO model and GRID partition technique	Tsinghua Tencent 100K dataset
Chiranjit et al.2019 [12]	Images	Traffic Sign Detection and data transmission	Based on Artificial Neural Network(ANN)	Using Vehicular Ad hoc Network(VANET)	Study specific dataset
Eminguney et al.2022 [14]	Real-time	Road objects, Traffic Sign Detection and recognition	Based on YOLO V5 architecture	Grid partition technique and CNN network	GTSRB and study specific dataset

G. Proposed Block Diagram

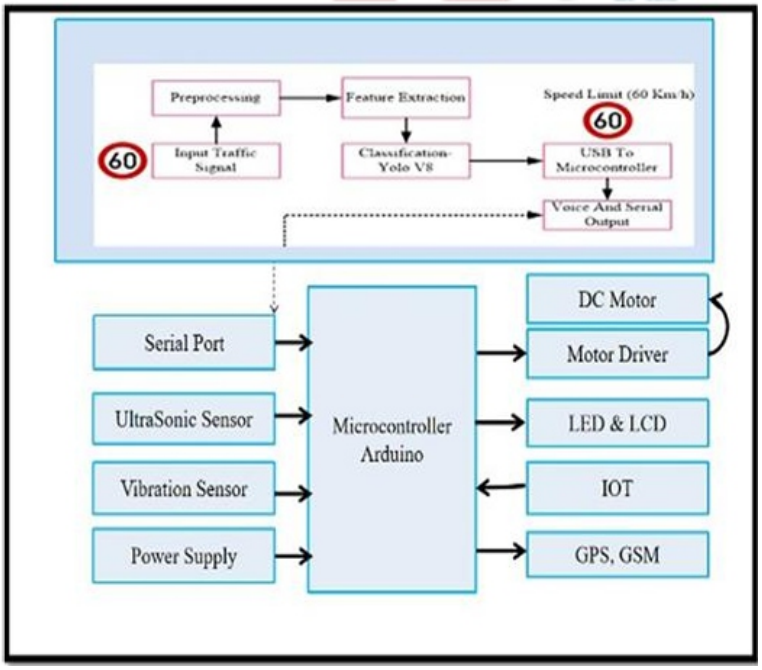

Fig. 4. Proposed Block Diagram

In this system, an automatic accident detection and avoidance of collision using advanced embedded technologies such as GSM MODEM, GPS and YOLO v8 technology. When the vehicle attained accident, vibration sensors are employed to detect the occurrence of accident and ultrasonic a sensor is utilized for detecting the obstacles or object. LCD display receives the command from the Arduino device. Automatically these signals send to the micro controller and immediately send to GPS section to gather the accident location. After all these process happens the micro controller sends the emergency signal to rescue unit through GSM module. The Blynk module acts as the user interface for the IoT system, offering a customizable platform for real-time monitoring and interaction. Through the Blynk mobile application, users can access various widgets to visualize data and control system functions remotely. With seamless integration and push notifications, users can monitor critical events, adjust settings, and track performance metrics for effective traffic safety management. From this system, we can able to reduce the accident rate and human death ratio by accidents. To develop a comprehensive hardware system, start by selecting a versatile micro controller board like Arduino or Raspberry Pi to serve as the central control unit. Integrate essential sensors such as an ultrasound sensor for obstacle detection, a GPS module for location tracking, and a GSM module for communication capabilities. Connect a motor driver to control movement through a DC motor, while incorporating an LCD display and LED for visual feedback. Additionally, incorporate a camera module to capture visual data, utilizing advanced computer vision techniques such as YOLOv8 for the detection and identification of objects. Ensure a stable power supply for consistent operation. Write code to initialize sensors, process inputs, and control outputs, enabling the system to respond intelligently to its environment and communicate data effectively. Thoroughly test the system to validate functionality across various scenarios, providing a versatile solution for diverse applications.

IV. RESULTS AND DISCUSSION

The implementation of YOLOv8 for traffic sign detection yielded promising results with enhanced accuracy, providing reliable identification of various traffic signs. Through rigorous testing in diverse environmental conditions, the system demonstrated improved performance in recognizing speed limit indicators, stop signals, and other critical traffic indicators. The integration of additional accuracy-enhancing techniques, such as fine-tuning model parameters and augmenting the training dataset, contributed to the overall robustness of the system. Furthermore, the integration of GPS and GSM modules facilitated the transmission of accurate location data and real- time alerts to mobile devices should a detected traffic sign. Leveraging GPS coordinates, the system not only sent messages containing latitude and longitude information but also calculated the distance to the detected sign, offering comprehensive situational awareness to driversAdditionally, the integration of ultrasonic sensors for identifying obstacles provided an extra layer of safety, thus allowing the system to identify and respond to potential hazards on the road. By incorporating obstacle detection capabilities alongside traffic sign recognition, the system demonstrated its versatility in addressing various safety concerns, further enhancing its practical utility in real-world scenarios. Overall, the successful integration of YOLOv8 traffic sign detection with GPS, GSM, and spotting obstructions technologies marks a notable advancement in in intelligent transportation systems. The combined capabilities ofaccurate sign detection, location-based alerts, and obstacle avoidance contribute to safer and more efficient road navigation, underscoring the potential of such integrated systems in enhancing overall road safety and driver experience. Continued research and development efforts in this area hold promise for further advancements and widespread deployment of intelligent transportation solutions.

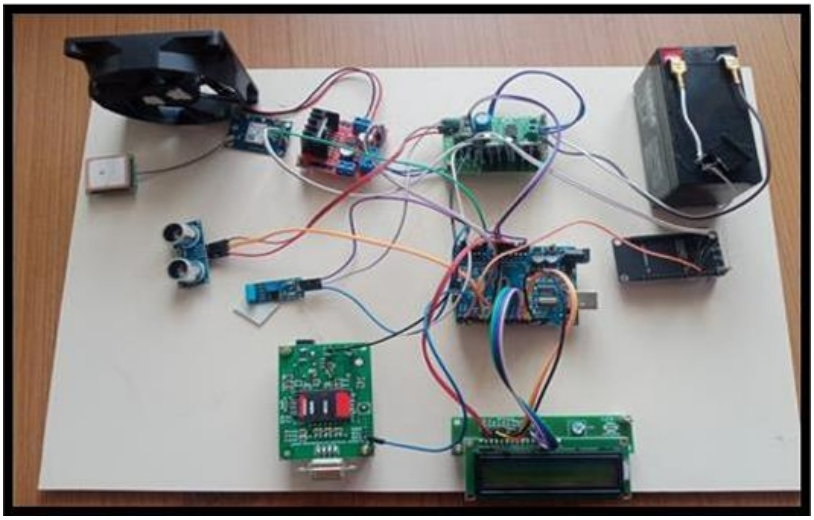

Fig. 5. Prototype Model of Proposed System

A. Vehicle Detection and Speed Control of Different Cases

YOLOv8, an upgraded version of the popular You Only Look Once (YOLO) object detection algorithm, could potentially offer better performance in accident detection and avoidance compared to its predecessors. Its improved architecture and optimization techniques can lead to faster and more accurate detection of objects, including vehicles, pedestrians, and obstacles, which are critical for accident prevention systems. Additionally, YOLOv8's ability to handle real-time processing makes it suitable for applications where quick detection and response are essential for avoiding accidents on the road.

In this study, we trained YOLOv8, a leading object detection algorithm, to accurately detect multiple traffic sign classes, including 30 km, 60 km, 80 km speed limit signs, school zone signs, and speed break signs. Leveraging a diverse dataset and transfer learning techniques, we fine-tuned the model to adapt to our specific detection task. Extensive testing demonstrated the model's robust performance in real- time detection across varied environments and lighting conditions, with minimal false positives and false negatives. The successful training of YOLOv8 offers promising prospects for integrating the model into intelligent transportation systems, enabling proactive response to traffic regulations and enhancing road safety. Future work entails further refining the model's performanceand scalability for real-world deployment in traffic management scenarios.

Case1: Vehicle Detect and control of Speed Limit for 30KM

To facilitate the detection and response to a "30 km" speed limit sign, integrate a camera module with the microcontroller board and utilize computer vision algorithms like YOLOv8 to analyze video frames and identify the sign. Once detected, adjust the motor speed via the motor driver to comply with the limit, while concurrently displaying a notification on the LCD screen for visual feedback. Thorough testing and refinement of the system are crucial to ensure precise sign detection and reliable adjustment of vehicle speed, contributing to enhanced safety and compliance with traffic regulations.

Fig. 6. Vehicle Detection of Control of Speed limit for 30KM

Case2: Vehicle Detect and control of Speed Limit for School Zone Area

In implementing a vehicle stoppage system for school zones through traffic sign detection, the focus lies on integrating a camera module with a microcontroller board. This setup allows for real-time processing of video frames to identify school zone signs or markings. Once the systemdetects the presence of a school zone sign, it triggers an immediate response to stop the vehicle. This response is typically achieved by sending a signal to the vehicle's braking system or motor control unit to halt the vehicle's movement.By leveraging computer vision algorithms and hardware integration, the system ensures timely and accurate detection of school zones, thereby enhancing safety in areas with a high concentration of pedestrians, such as school zones.

Fig. 7. Vehicle Detection of Control of Speed limit for School Zone

Case3: Vehicle Detect and control of Speed Limit for 80KM

To facilitate the detection and response to a "30 km" speed limit sign, integrate a camera module with the microcontroller board and utilize computer vision algorithms like YOLOv8 to analyze video frames and identify the sign. Once detected, adjust the motor speed via the motor driver to comply with the limit, while concurrently displaying a notification on the LCD screen for visual feedback. Thorough testing and refinement of the system are crucial to ensure precise sign detection and reliable adjustment of vehicle speed, contributing to enhanced safety and compliance with traffic regulations.

Fig. 8. Vehicle Detection of Control of Speed limit for 80 KM

Case4: Vehicle Detect and control of Speed Limit for Speed Breaker

Fig. 7. Vehicle Detection of Control of Speed limit for School Zone This study integrates the YOLOv8 algorithm for real-time speed breaker detection in vehicles. Upon identification, the system halts the motor and displays "Speed Breaker" on the LCD for driver awareness. By leveraging YOLOv8's capabilities, drivers are alerted to road hazards, enhancing road safety. Thorough testing guarantees dependable operation across various conditions, improving overall driving experiences.

Fig. 9. Vehicle Detection of Control of Speed limit for Obstacles

B. Accident Detection

This study presents the creation of an accident detection system integrating a vibration sensor, liquid crystal display (LCD) screen, global system for mobile communications (GSM) module, and Blynk app. When significant vibrations indicating an accident are detected, the system displays "AD" on the LCD, sends an SMS containing latitude and longitude coordinates, along with the distance to a predefined mobile number by GPS and GSM, and updates the Blynk app status to "1" by IOT. The distance calculation is based on comparing the current GPS coordinates with the coordinates of a predetermined location, such as the user's home or workplace. Conversely, in normal conditions, it displays "AN" on the LCD and updates the Blynk app status to "0". Through hardware and software integration, the system enhances road safety by promptly alerting authorities and drivers to potential accidents, facilitating swift emergency response measures.

Fig. 10. Vehicle Accident Detection and Remedial Action

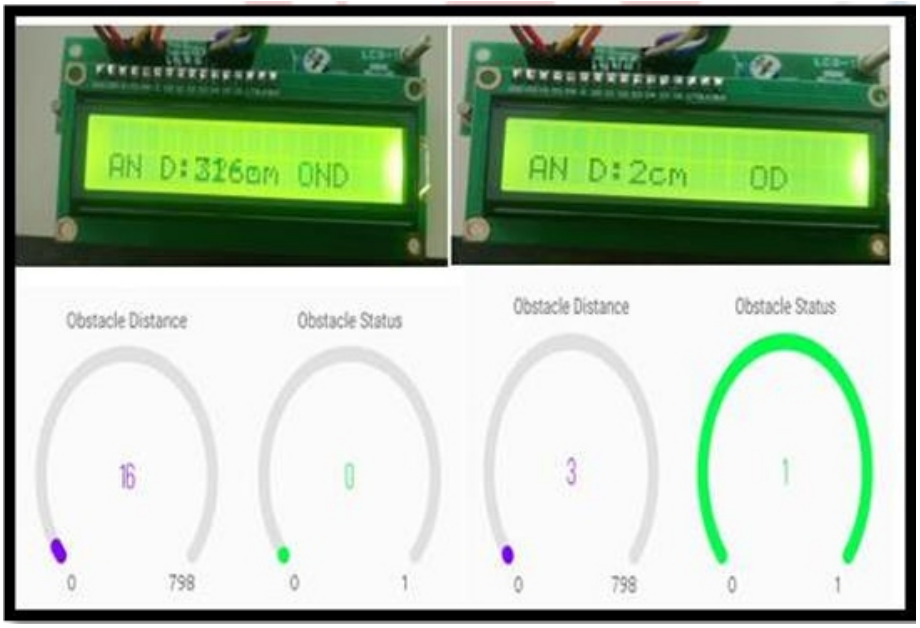

Fig. 11. Safety Measures: Obstacle Detection and Response

C. Obstacle Detection and Collision Avoidance

This study introduces a live, real-time obstacle detection system leveraging an ultrasonic sensor and Blynk app integration for enhanced vehicle safety. When obstructions are identified within 10 meters, the LCD displays "OD" with the distance, and the Blynk app updates accordingly.Conversely, when no obstacles are detected, "OND" is displayed on the LCD and the Blynk app status remains unchanged. This integrated approach ensures proactive obstacle avoidance measures and enhances driver awareness, contributing to safer navigation in dynamic environments.

V. CONCLUSION

The proposed system represents a pioneering integration of cutting-edge technologies aimed at revolutionizing road safety and traffic management. By combining advanced deep learning- based detection techniques with micro controller-based speed control and accident detection systems, the solution addresses key challenges in contemporary transportation systems. Leveraging the power of state-of-the-art YOLO v8 models for traffic sign detection, the system ensures accurate and real-time identification of traffic signs, enabling proactive responses to changing road conditions and speed limits. Additionally, the micro controller-based speed control module dynamically adjusts vehicle velocity in accordance with detected speed limits, thereby enhancing driver compliance and overall safety on the road. Furthermore, the incorporation of GPS and vibration sensors in the accident detection system enables timely detection and response to potential collisions or accidents, ensuring the swift deployment of emergency protocols and assistance. Seamless data transmission via ESP8266 Node MCU GSM GPS enhances communication between system components, facilitating real-time monitoring and control through the user-friendly interface provided by the Blynk app. This comprehensive strategy not only improves road safety but also enhances traffic flow and management efficiency. Looking ahead, future efforts will focus on expanding the dataset to improve model accuracy and exploring innovative methods to further enhance detection speed and precision in real-world scenarios, ultimately advancing the capabilities of the suggested system and its impact on transportation safety and efficiency.

VI. ACKNOWLEDGEMENT

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Deep Learning Model for Plant Leaf Disease Classification using Double Gan

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ABSTRACT

Traditional plant disease diagnosis methods primarily rely on visual inspection, which can be limited in accuracy and scalability. To address these challenges, this study introduces a novel framework leveraging Double GAN, a generative adversarial network, to generate synthetic diseased leaf images. This approach helps overcome imbalanced datasets commonly encountered in plant disease datasets. The synthetic images, combined with real ones, are utilized to train a deep learning model, achieving an impressive accuracy of 99.80% in disease classification tasks. Furthermore, the framework integrates recommendations for preferred pesticides based on the identified disease, enabling targeted action and potentially reducing the reliance on broad-spectrum options. This innovative approach underscores the effectiveness of deep learning coupled with data augmentation techniques for accurate plant disease detection. It also provides valuable insights for promoting sustainable crop protection practices, highlighting the potential of advanced technologies in agricultural sustainability and productivity.

Keywords— Plant diseases, deep learning, Double Generative Adversarial Network (Double GAN), Data Augmentation, Image Classification, Sustainable Agriculture, Pesticide Recommendation.

I. INTRODUCTION

India, as an emerging economy, has traditionally heavily depended on agriculture as a primary income source for a significant portion of its population. However, the agricultural sector encounters various challenges, including substantial crop production losses in crop fields. Among these challenges, identifying plant leaf diseases emerges as a critical issue. Early detection of leaf diseases is crucial to prevent their spread to other plants, ensuring yield protection and averting financial losses for farmers. The consequences of plant leaf diseases can vary from minor disruptions to the complete devastation of entire plantations, significantly impacting the agricultural economy.In essence, effective management of plant leaf diseases is essential for sustaining agricultural productivity and ensuring the economic well-being of farmers in India.[1],[2],[3]. The integration of computer vision into precision agriculture presents an opportunity to significantly improve disease identification efficiency. Harnessing computer vision technologies can enhance the accuracy and precision of disease identification, providing a streamlined alternative to manual approaches.[4], [5].

Agriculture stands as a pivotal profession in developing nations such as India, playing a vital role in shaping the economy. Crop losses significantly impact a nation's financial stability. This can lead to famines and heightened unemployment rates within the agricultural sector. A key hurdle in combating plant illnesses and mitigating crop loss is the imperative for increased awareness among farmers. [6],[7],[8]. The Double GAN algorithm utilizes generative adversarial networks (GANs) to detect subtle patterns and anomalies associated with plant diseases. Deploying this algorithm in crop fields enables early disease detection, aiding farmers in proactive intervention to prevent disease spread and minimize crop losses. Moreover, the algorithm's adaptive nature allows it to learn and adjust to new disease strains, ensuring reliable performance across different environments and crop types. Besides disease detection, analyzing soil nutrient deficiencies is crucial. Tailoring fertilizer applications to address deficiencies in essential nutrients like nitrogen, phosphorus, potassium, zinc, and iron can enhance plant immunity, promote recovery from diseases, and optimize overall crop yields.

II. LITERATURE REVIEW:

The issue of uneven sample distribution was addressed in the PlantVillage database concerning leaf disease identification, utilizing methods such as flipping and translation to complement the dataset. Compared to regularization and other techniques, expanding the original dataset can significantly enhance model performance and mitigate overfitting risks.Furthermore, a rapid and reliable approach to quantify lesions using image recognition and an artificial neural network model was developed. These disease recognition methods have demonstrated promising results.This section delves into the literature surrounding the detection and classification of plant or crop diseases. Ashwin Kumar proposed an Optimal Mobile Network-based Convolutional Neural Network (OMNCNN) for the recognition and categorization of plant leaf diseases, incorporating phases such as pre-processing, segmentation, feature retrieval, and categorization. Bedi and Gole introduced a hybrid approach combining a Convolutional Auto Encoder (CAE) and Convolutional Neural Network (CNN) structure for autonomous plant disease diagnosis. Rahman et al. presented an advanced recognition and categorization approach based on deep learning (DL) models for effective disease identification tasks.

III. PROPOSED METHODOLOGY

Innovating a comprehensive system for detecting various diseases across various places is complex by visualizing agricultural fields manually for the symptoms of affecting leaves consumes much time too and analyzing the fertilizers is hard to implement to overcome these issues a new deep learning method is proposed for detecting, categorizing and fertilizer recommendation for the affected leaf. It consist of 4 steps,

That are, (i) Pre-processing (ii) Segmentation (iii) Feature Extraction (iv) Classificationthese techniques are briefly explained below.

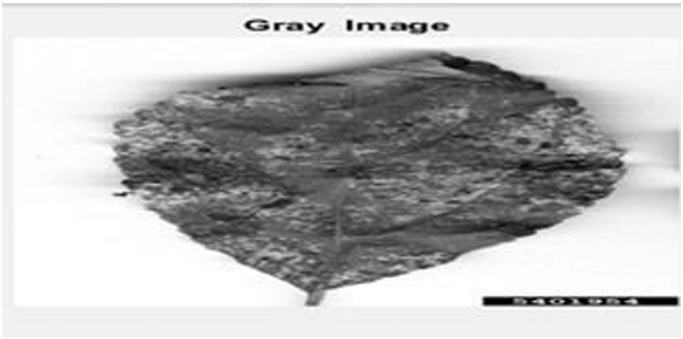
Step 1: Pre-Processing

Preprocessing in image processing encompasses a range of techniques designed to ready images for analysis or subsequent processing. It encompasses diverse operations aimed at boosting image quality, diminishing noise, and extracting pertinent information. Typical preprocessing steps comprise resizing, denoising, normalization, cropping, rotation, color space conversion, and histogram equalization. These methodologies contribute to enhancing the efficiency of subsequent image processing tasks such as segmentation, feature extraction, and object recognition. The preprocessing process is typically divided into three phases: (I) converting the image to grayscale, (ii) enhancing contrast, and (iii)

converting the image from RGB format.
% Step 1 - Preprocessing
%ImageResize ReI = imresize(I,[256 256]);
%figure;imshow(ReI);
title ('Resized Test Image');

1. Gray Scale Conversion:

Converting an image to grayscale involves transforming a color image into a black-and-white version, where each pixel denotes only its brightness value. This conversion is achieved by averaging the color channels or applying specific coefficients to compute luminance. Grayscale images are less complex and demand less memory, rendering them valuable for tasks such as image analysis and computer vision.

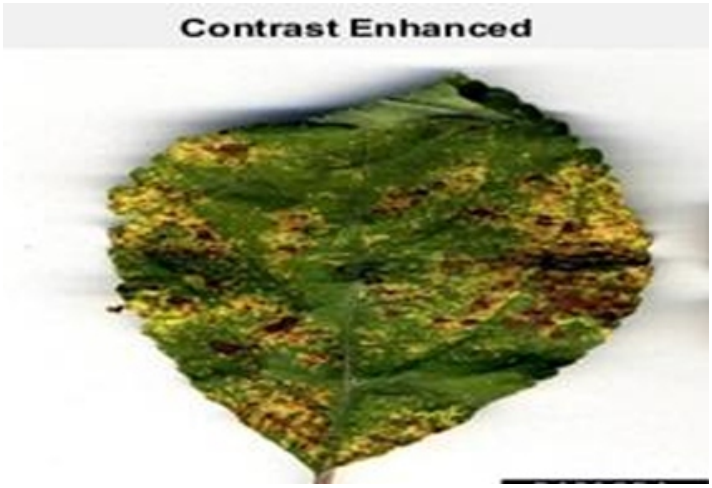


% Gray Conversion

GrI = rgb2gray(ReI);
figure; imshow(GrI);
title ('Gray Image');

2. Contrast enhancement:

In image processing, contrast enhancement involves employing methods to heighten the visual contrast between distinct regions of an image by amplifying the intensity disparity among them. The objective is to intensify dark areas while brightening lighter areas, ultimately augmenting overall contrast and highlighting finer details within the image.Top of Form



% Noise Removal and Filtering

```
NrI = imadjust(ReI,stretchlim(ReI));
figure, imshow(NrI);title('Contrast Enhanced');
```

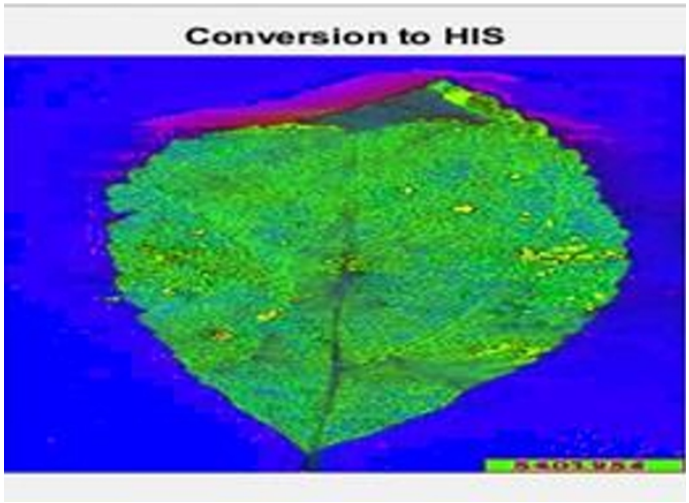
3. Converting an image from RGB:

Converting an image from RGB (Red, Green, Blue) color space to HIS (Hue, Intensity, Saturation) color space involves transforming the pixel values to represent these three components. Here's a brief explanation of the transformation:

Hue (H): Represents the dominant wavelength of color. It is typically measured in degrees ranging from 0 to 360, with 0 and 360 both representing red, 120 representing green, and 240 representing blue.

Intensity(I): It represents the brightness or luminance of color and is determined as the mean of the three RGB components, usually normalized within the range of [0, 1].

Saturation (S): Represents the purity or vividness of the color. It measures the distance of the color from a neutral gray of equal intensity. Saturation valvalues range from 0 (neutral gray) to 1 (fully saturated color).



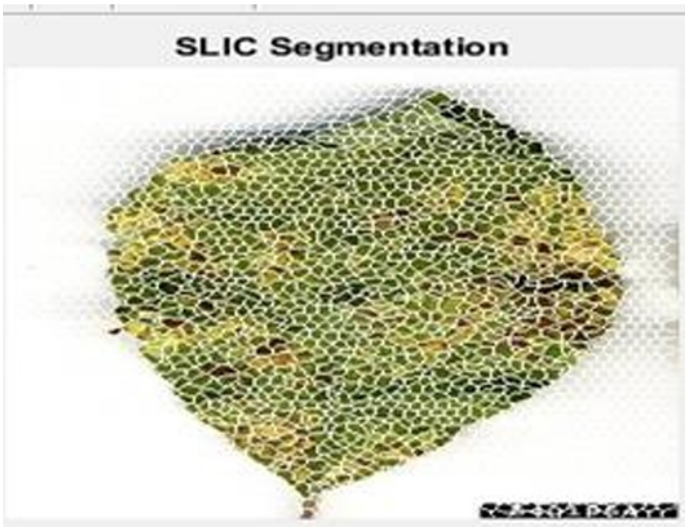
% Conversion to HIS

```
I_HIS = rgb2hsi(NrI);
figure,imshow(I_HIS);
title('Conversion to HIS);
```

Step 2: Segmentation

SLIC (Simple Linear Iterative Clustering) segmentation is a method used to divide an image into compact and uniform regions called superpixels. It works by initializing cluster centers across the image, assigning pixels to the nearest cluster based on color and spatial proximity, and iteratively refining the clusters until convergence. SLIC is efficient, producing uniform superpixels suitable for various computer vision tasks.

For best outcomes, it may be necessary to choose parameters and apply post-processing techniques during the detection and classification of crop diseases. Utilizing DL, ML, and computer vision techniques is crucial in the agricultural sector [1]. The objective is to create algorithms and methods using leaf or plant feature images for automatic detection and classification of plant diseases, aiding farmers in disease management. After thoroughly examining various recent ML and DL-based approaches,



% SLIC

```
[Ni, l, Am, C] = slic
(NrI, 3000, 10, 1, 'median');
figure;
imshow(drawregionboundaries(l, NrI, [255 255 255]));
title('SLIC Segmentation');
```

Step 3: Feature Extraction

Feature extraction, a core concept in image processing, computer vision, and machine learning, involves identifying and capturing pertinent information or patterns from raw data like images, creating a more concise and meaningful representation. In the HIS (Hue, Intensity, Saturation) color space, the hue component segregates color information independently of brightness (intensity) and colorfulness (saturation). By extracting the hue image, we isolate this hue information from the original image, emphasizing the color characteristics of the scene.

(I) Hue image:

The "Hue image" refers to an image representation where each pixel's value represents the hue component of its corresponding pixel in the original image The literature on plant disease detection and classification has highlighted several challenges, aiding researchers in exploring factors that can significantly affect real-time systems for plant identification and diagnosis. Various factors and issues can impact disease identification and classification, driving further investigation and innovation in this field.

Hue represents the dominant wavelength of color, essentially indicating the color tone or "pure" color of the pixel, irrespective of its brightness or saturation.

(ii) Saturation Image:

The "saturation image" is an image representation where each pixel's value represents the saturation component of its corresponding pixel in the original image. Saturation measures the intensity or purity of a color, indicating how vivid or intense the color appears, independent of its brightness or hue.

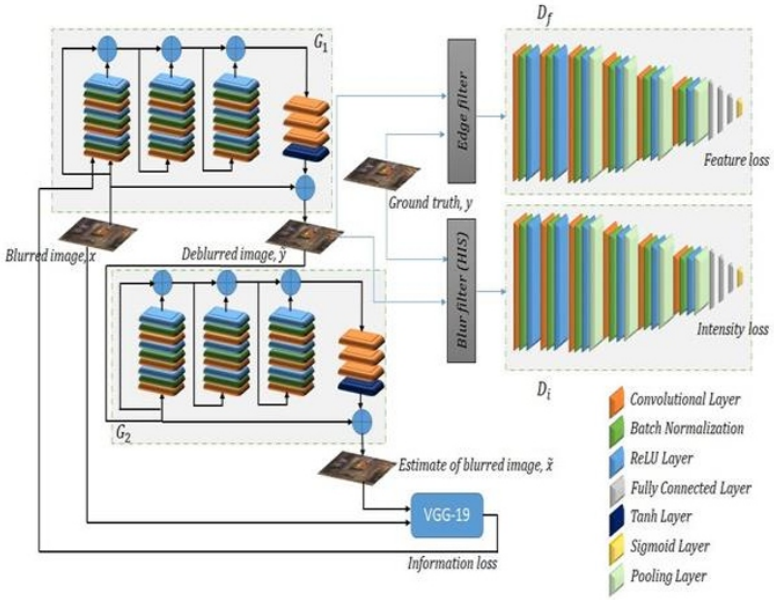
(iii) Intensity Image:

The "intensity image" is a representation of an image where each pixel's value represents the intensity component of its corresponding pixel in the original image. Intensity refers to the brightness or luminance of a pixel, independent of its information.

% Extract out the H, S, and V images individually

```
hImage = I_HIS(:,:,1);
sImage = I_HIS(:,:,2);
iImage = I_HIS(:,:,3);
figure;
subplot(1,3,1); imshow(hImage); title('Hue Image');
subplot(1,3,2); imshow(sImage); title('Saturation Image');
subplot(1,3,3); imshow(iImage); title('Intensity Image');
set(gcf, 'units','normalized','outerposition',[0 0 0.9 0.9]);
addpath(genpath('seg'));
NrI = imresize(I, [256 256]);
```

STEP 4: CLASSIFICATION



Network Architecture of DoubleGAN Algorithm

The Concept Behind Doublegan:

The training process involved separate training of the WGAN in stage I and the SRGAN in stage II. Once the training was finished, random noise served as input, and the generated network segments from stages I and II were extracted individually and subsequently linked in sequence.

First Stage of GAN

The first stage of GAN was used to generate a clear, lowresolution 64*64 image. Unlike in the traditional GAN, the loss of the discriminator was the Wasserstein distance between the generated data and the real data, which is defined as:

$$W(P_{data}, P_G) = \max_{D \in 1-Lipschitz} \{E_{x \sim P_{data}}[D(x)] - E_{x \sim P_G}[D(x)]\} \quad (1)$$

In equation (1), x represents the real image from the data distribution pdata;D represents the discriminator network, G represents the generator network, and E represents the expected value. Unlike traditional GANs that use JS divergence, where the overlap between pdata and PG can be ignored or non-overlapping parts, resulting in a constant value (log 2) and gradient disappearance issues, the Wasserstein distance addresses this by accurately reflecting the distance between pdata and PG even when there is no overlap. This stabilizes training, preventing model collapse due to gradient disappearance, making it advantageous for training GANs effectively.

The Second Stage of the GAN:

In the second stage, the input images generated in the first stage are processed through the SRGAN to super-resolution reconstruct low-resolution input images, resulting in clear, high-resolution plant leaf images. The GAN framework aims to minimize perceptual losses by modeling based on Mean Squared Error (MSE), which compensates for the lack of detail. The loss function is structured as:

$$l^{SR} = l_X^{SR} + a l_G^{SR} \quad (2)$$

Equation (2) defines IXSR as the content loss, RGSR as the adversarial loss, and a as the adversarial loss weight, set to 10-3 in this experiment. The content loss, employing MSE loss, ensures consistent content alignment between the generated image and the original image. This loss is calculated as pixel-level loss between the super-resolution image and the real image.

$$l_{MSE}^{SR} = \frac{1}{r^2 WH} \sum_{x=1}^{rW} \sum_{y=1}^{rH} (I_{x,y}^{HR} - G(I^{LR})_{x,y})^2 \quad (3)$$

Equation (3) introduces r as the down-sampling factor, while W and H represent the width and height of the image, respectively. To address the absence of high-frequency details in images generated by MSE a ReLU layer from the pre-trained VGG 16 model was utilized. Subsequently, both the generated and matched real images were fed into the VGG model, extracting characteristic pixels from the middle layer of both images and computing the Euclidean distance between them. The formula is expressed as follows:

$$l_{YGG}^{SR} = \frac{1}{W_{i,j} H_{i,j}} \sum_{x=1}^{W_{i,j}} \sum_{y=1}^{H_{i,j}} ((\emptyset_{i,j}(I^{HR}))_{x,y} - (\emptyset_{i,j} G(I^{LR}))_{x,y})^2 \quad (4)$$

quation (4) introduces Wi, j and Hi, j as the height and width of the extracted feature surface, respectively. The adversarial loss was employed to ensure that the generated image belonged to the natural image domain, effectively preventing the discriminator from distinguishing between images originating from either the generated or real image sources. This concept is illustrated as follows:

$$l_G^{SR} = \sum_n^N = -\log D\,(G(I^{LR})) \quad (5)$$

Equation (5) describes D(G(ILR) as the probability estimation of the discriminator D for the super-resolution image G(ILR). This arrangement is designed to optimize gradient performance.

```
% % ANN Clasification
fprintf('Loading Data...\n')
load('CNN_Data.mat');
fprintf('Data Loaded Successfully...\n')
inputs = X_cent_1'; %512 features
load('CNN_Label.mat')
test_x = cnn_net(Ni);
train_cnn = mean(X_cent_1,2);
test__cnn  = mean(test_x,2);
cnn_data = ismember(train_cnn, test__cnn);
cnn_mem  = find(cnn_data(:,1)>0);
fprintf('* * * * Affected Disease * * * * \n')
if (cnn_mem >= 0) && (cnn_mem <= 5)
% % Mosaic disease
disp('1. Mosaic')
helpdlg({'  Disease Name: Mosaic'.
'Fertilizer: MICRONUTRIENT NUTRITION'});
fprintf(S,'%s','1');
elseif (cnn_mem >= 16) && (cnn_mem <= 20)
% % Marssonina Leaf disease
disp('2. Marssonina Leaf')
helpdlg({'  Disease Name: Marssonina Leaf  '...);
'Fertilizer: PHOTOSYNTHETIC NUTRITION'});
fprintf(S,'%s','2');
elseif (cnn_mem >= 21) && (cnn_mem <= 25)
% % Anthracnose disease
disp('3. Anthracnose Disease')
helpdlg({'  Disease Name: Anthracnose Disease  '...
'Fertilizer: Nitrogen Fertilizer'});
fprintf(S,'%s','3')
elseif (cnn_mem >= 26) && (cnn_mem <= 30)
% % Bacterial Leaf Spot Disease
disp('4. Bacterial Leaf Spot Disease') helpdlg({'  Disease
Name: Bacterial Leaf Spot Disease '...
'Fertilizer:  Sulfur Sprays, Neem Oil'});
fprintf(S,'%s','4');
elseif (cnn_mem >= 31) && (cnn_mem <=            35)
```

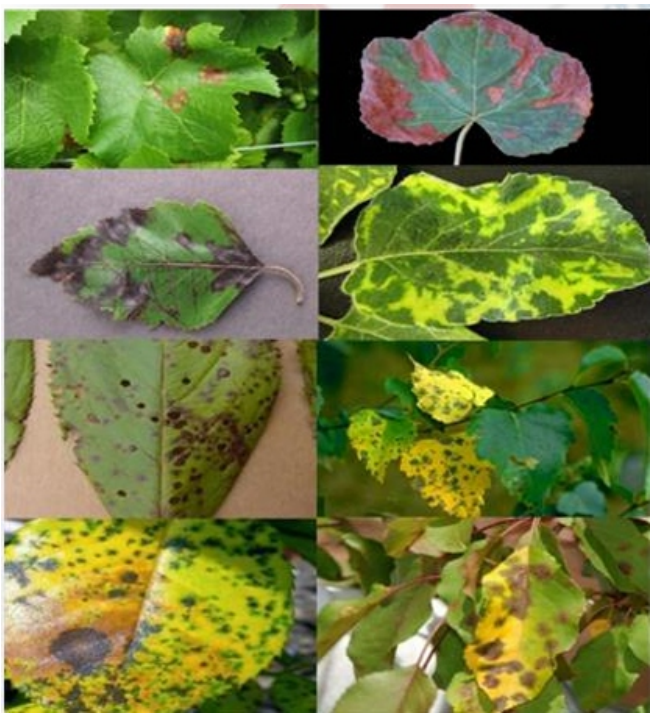
```
% % Downy Mildew disease
disp('5. Downy Mildew');
helpdlg({'  Disease Name: Downy Mildew  '...
'Fertilizer: Copper Spray'});
fprintf(S,'%s','1');
elseif (cnn_mem >= 46) && (cnn_mem <= 50)
disp('6. Rust Disease ')
helpdlg({'  Disease Name: Rust Disease   '...
'Fertilizer: Scotts Turf Builder Lawn Food'});
fprintf(S,'%s','2');
elseif (cnn_mem >= 61) && (cnn_mem <= 65)
% % Cercospora Leaf Spot Disease
disp('7. Cercospora Leaf Spot Disease')
helpdlg({'  Disease Name: Cercospora Leaf Spot   Disease
'... 'Fertilizer: Cultural Controls - ammonium nitrate,
ammonium sulfate, or quick-release urea formulation '});
fprintf(S,'%s','3');
elseif (cnn_mem >= 76) && (cnn_mem <= 82)
disp('16. Normal')
helpdlg('  Normal  ');
else
disp('No')
end
```

Proposed Block Diagram:

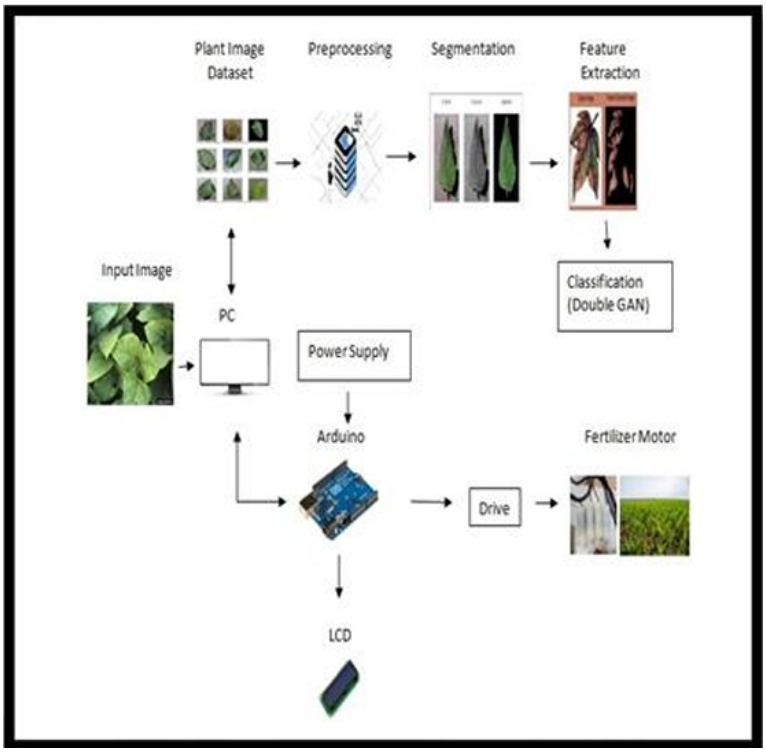
The proposed block diagram presents a sophisticated system designed to address the pressing need for efficient plant disease detection and treatment in agriculture. At its core, the system leverages advanced technologies such as image processing, microcontroller-based control, and mechanical actuation to provide a holistic solution for farmers and agricultural practitioners. Starting with the initial input of plant leaf images from a dataset, the system embarks on a journey of analysis and action. The preprocessing steps carried out on a personal computer (PC) play a crucial role in enhancing the quality of the input images, preparing

them for subsequent stages of analysis. These preprocessing steps may include operations such as noise reduction, contrast enhancement, and image normalization, all aimed at optimizing the data for accurate segmentation and feature extraction.

After the preprocessing stage, segmentation follows, which involves dividing an image into meaningful regions. This segmentation allows the system to concentrate its analysis on relevant parts of plant leaves, ultimately enhancing the accuracy and efficiency of disease detection.



Sample Results for Detecting the leaf disease using DoubleGAN



Feature extraction, a pivotal component of the system, relies on the capabilities of an Arduino board interfaced with a power supply and an LCD display. The Arduino board serves as the computational heart of the system, executing algorithms to extract discriminative features from the segmented leaf images. These features may include texture patterns, color distributions, or morphological characteristics indicative of specific diseases or health conditions in plants. The integration of an LCD display into the system provides real-time feedback to the user, enhancing the transparency and usability of the automated process. Through the display, farmers can monitor the progress of the disease detection and treatment stages, gaining insights into the health status of their crops. The display also serves as a user interface, facilitating interaction with the system and enabling adjustments or interventions as needed. The subsequent stage of the system involves the deployment of mechanical actuators, specifically four motors, for targeted treatment of diseased plant leaves. These motors, controlled by the Arduino board, enable precise and localized application of fertilizers or other therapeutic agents to the affected areas, minimizing waste and maximizing efficacy. By automating the treatment process, the system streamlines agricultural operations, freeing up valuable time and resources for farmers to allocate elsewhere. The pump display stage, which briefly illuminates to indicate the activation of the pump for fertilizer application, serves as a visual confirmation for the user. However, recognizing the potential need for extended display time to accommodate varying user preferences and operational requirements, the system offers flexibility in adjusting the duration of the display. This adaptability enhances the user experience and ensures that the system aligns with the diverse needs of its users across different agricultural contexts.

IV. RESULT & DISCUSSION

During the data collection phase, gather a substantial dataset comprising images of both healthy and diseased plant leaves, ensuring diversity across plant species and diseases. Standardize the images through preprocessing, which may involve resizing, normalization, and augmentation to enhance dataset variability. Subsequently, train the Double GAN model using the preprocessed dataset. This model comprises two neural networks, a generator, and a discriminator, trained concurrently in a competitive framework. In detection phase once the Double GAN model is trained, deploy it in crop fields or greenhouse environments where plant health monitoring is required. Capture images of plant leaves using cameras or drones. Image analysis process the images captured in the field through the trained Double GAN model. The model will analyze the images and identify any subtle patterns or anomalies indicative of plant diseases. At the result Interpretation that based on the analysis, the Double GAN algorithm will provide a diagnosis for each plant leaf image, indicating whether it is healthy or diseased.

Accuracy: Evaluate the accuracy of disease detection achieved by the Double GAN algorithm compared to traditional methods. Discuss any improvements or limitations observed.

Early Detection: Highlight the advantage of early disease detection enabled by the Double GAN algorithm. Discuss how early detection can help farmers take proactive measures to prevent the spread of diseases and minimize crop losses.

Cost-effectiveness: Consider the cost-effectiveness of implementing Double GAN technology for disease detection in crop fields. Compare the cost of implementation to potential benefits such as increased crop yield and reduced pesticide usage.

CASE 1: Disease Detection in Apple Plant Leaf Affected by Mosaic Disease

In Case 1, we utilized Double GAN technology for the detection of mosaic disease in apple plant leaves. Mosaic disease is a common viral infection characterized by distorted leaf patterns and reduced yield in apple crops. The goal of this study was to leverage the power of generative adversarial networks (GANs) within the Double GAN framework to accurately detect subtle patterns and anomalies indicative of mosaic disease in apple plant leaves.In the Data Collection and Preprocessing, we collected a comprehensive dataset comprising images of healthy apple plant leaves and leaves affected by mosaic disease. These images were preprocessed to standardize dimensions, normalize colors, and augment dataset diversity.

Plant Sample	Disease affected	Fertilizer Recommended
	Mosaic	Micronutrient nutrition

The Double GAN model was trained on the preprocessed dataset. This model consists of two neural networks, a generator and a discriminator, trained simultaneously in a competitive setting to generate realistic images of both healthy and diseased apple plant leaves. Based on the analysis, the Double GAN algorithm provided a diagnosis for each apple plant leaf image, indicating whether it was healthy or affected by mosaic disease. Case 1, demonstrated the efficacy of using Double GAN technology for early detection of mosaic disease in apple plant leaves, with practical implications for precision agriculture and disease management strategies. Additionally, the recommendation of the "Micronutrient Nutrition" fertilizer for the affected plant leaf.

CASE 2: Disease Detection in Aspen Plant Leaf Affected by Marssonina Disease

The application of Double GAN technology for the early detection and management of Marssonina leaf disease in aspen plants. Marssonina leaf disease poses a significant threat to aspen forests, leading to defoliation and reduced tree health. Therefore, there is a need for advanced technologies that can accurately identify and diagnose Marssonina leaf disease in its early stages. In this case study, Double GANtechnology is employed to analyze images of aspen leaves and detect subtle patterns indicative of Marssonina leaf disease. In data collection and preprocessing, the first step in the case study involves the collection of a comprehensive dataset comprising images of healthy aspen plant leaves and leaves affected by Marssonina leaf disease. These images are collected from aspen forests and undergo preprocessing to standardize dimensions, normalize colors, and augment dataset diversity.

Plant Sample	Disease affected	Fertilizer Recommended
	Marsssonina leaf	Photosynetic nutrition

Preprocessing techniques such as resizing, color normalization, and data augmentation ensure that the dataset is suitable for training the Double GAN model and enhances its ability to generalize across different lighting conditions, angles, and variations in leaf appearance. In detection phase, after training, the Double GAN model is deployed in aspen forests to capture images of plant leaves using cameras or drones. These images are then processed through the trained model to analyze and identify subtle patterns indicative of Marssonina leaf disease.

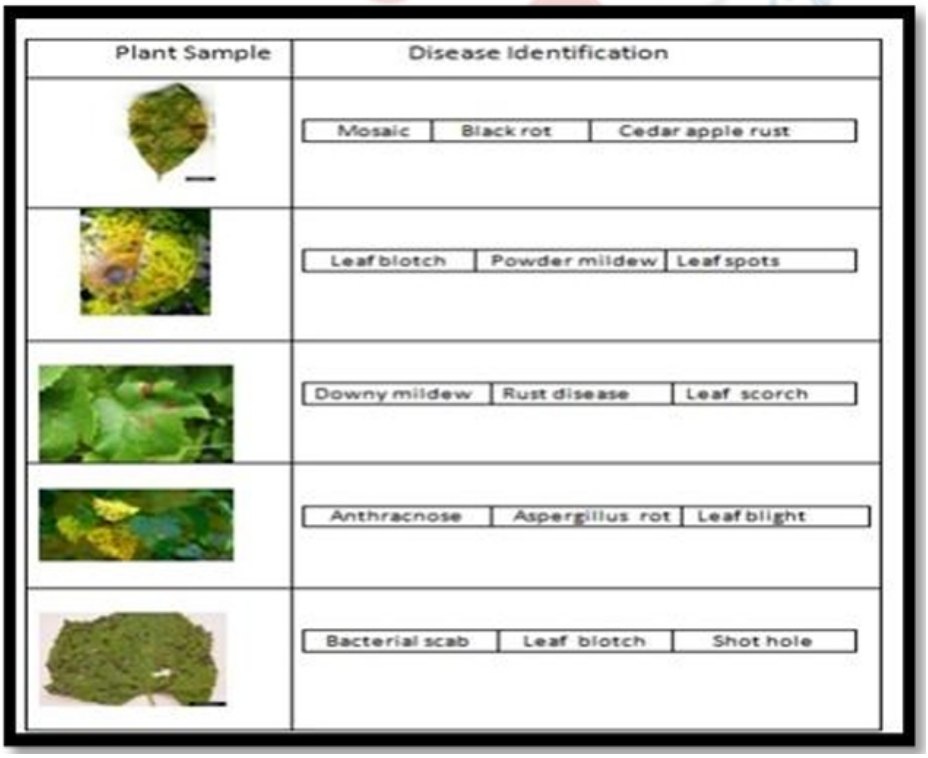
CASE 3: Disease Detection in Cineraria Plant Leaf Affected by Downy mildew Disease

The application of Double GAN technology for the early detection and management of downy mildew in cineraria plants. Downy mildew is a common fungal disease that poses a significant threat to cineraria plants, leading to leaf discoloration, wilting, and reduced plant vigor. Traditional methods of disease detection often rely on visual inspection, which may not be sensitive enough to detect early signs of infection. In this case study, Double GAN technology is employed to analyze images of cineraria leaves and detect subtle patterns indicative of downy mildew.

Plant Sample	Disease affect	Fertilizer Recommended
	Downy Mildew	Copper Spray

In data collection and preprocessing, the first step in the case study involves the collection of a comprehensive dataset comprising images of healthy cineraria plant leaves and leaves affected by downy.

Images of Different Plants Dataset:



Mechanism:

Pre-Treatment Plant Dataset Vs Post- Treatment Plant Dataset:

The pre-treatment dataset consists of images or data points of plants affected by various leaf diseases. Giving proper fertilizer or treatment, the post-treatment dataset consists of images or data points representing the same plants after they have healed or improved in health. The dataset reflects plants that have shown,

Unaffected vs Affected leaf

Pre LED stage Vs Post LED stage:

Prior to treatement, the LED display remains inactive and does not convey any information. In the post-treatment stage, the LED display is activated to indicate the status of the pump stage, displaying details on which pump is to be opened or closed. Information on the activation status of the pump stage (open/close) is display in the LED screen.

Pre-processing stage of Motor Vs post-processing stage of Motor:

In the pre-processing stage the motor is inactive, indicating that the system is idle and not currently spraying fertilizer. When the process is activated it triggered by some condition (e.g., detection of disease-affected plants, a timer, manual activation), the motor starts its process. The motor begins operating to drive the pump. Based on the specific requirements (such as the type of plants, area to cover, severity of the disease, etc.), valves controlling the flow of fertilizer are opened. Fertilizer is sprayed onto the plants via the pump and the opened valves. The spraying continues for a specific time period.After the process Completed the predefined time period for spraying fertilizer is complete, the motor and pump stop operating.

Based on your setup requirements, consider incorporating sensors to detect diseases, timers to regulate spraying duration, and control systems to manage motor, pump, and valves operations. It is essential to implement safety measures to ensure accurate fertilizer application and to safeguard plants and the environment from harm.

V. CONCLUSION:

Our project integrates MATLAB preprocessing techniques, including DoubleGAN segmentation, with an Arduino-based automated fertilizer application system to revolutionize plant disease management in agriculture. Initially, MATLAB preprocesses input leaf images, enhancing quality and consistency through noise reduction and contrast enhancement. This preparatory step optimizes subsequent analyses, ensuring accurate disease detection and treatment. Segmentation, facilitated by the advanced DoubleGAN algorithm, precisely delineates diseased regions within plant leaves. By isolating affected areas, DoubleGAN enhances discrimination between healthy and diseased tissues, facilitating targeted intervention. This segmentation accuracy forms the basis for effective treatment strategies, crucial for optimizing crop health and productivity. The Arduino-based control system serves as the project's core, coordinating automated fertilizer application to identified diseased areas. Interfaced with relay motors, the Arduino board orchestrates fertilizer dispensation based on segmented leaf regions. This real-time control mechanism ensures precise and timely treatment delivery, minimizing resource wastage while maximizing treatment efficacy. In practical terms, our system provides substantial benefits for agricultural practitioners. By accurately detecting and treating diseased leaves, it mitigates crop losses and enhances overall yield potential. This is especially impactful in large-scale agricultural operations, where even marginal improvements in crop health translate to substantial productivity gains. Additionally, the user-friendly interface empowers farmers to manage plant diseases effectively, simplifying complex agricultural tasks and enabling informed decision-making regarding crop health management. Moreover, by leveraging cutting-edge technologies such as MATLAB and Arduino, our project contributes to the digital transformation of agriculture. Through computational algorithms and real-time control systems, we enhance agricultural efficiency, sustainability, and resilience. Ultimately, our project represents a pivotal advancement in sustainable agricultural development, offering a transformative solution for addressing plant diseases and optimizing crop yields in modern farming contexts.

VI. ACKNOWLEDGEMENT

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Secure 16-bit Low Power Linear Feedback Shift Register for Advance Communication System at 90nm Technology

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ABSTRACT

To move a data word's bit position to the left or right, utilize a shift register. The brief proposes XOR gate, NOT gate as feedback latch based linear shift register. This paper presents a high secure linear feedback shift register, which can perform both serial and parallel operations. They reduce the power consumption and delay by replacing gate as feedback with the proposes based latch. The proposes 16-bit linear feedback shift register were simulated using 90nm CMOS process. A linear feedback shift register (LFSR) has been studied in this paper XOR gate and NOT gate use as feedback for enhancement of security purpose. They consume power 94.59% and 95.16% and reduce delay 86.72% and 27.40% with Vdd= 1.8V and a clock frequency of 100MHz.

Index Terms— Low Area, Low Power, Shift Register, Short Delay, Power Delay Product (PDP), XOR Feedback

I. INTRODUCTION

Linear Feedback Shift Registers (LFSR) are crucial com- ponents in many applications, particularly in the field of digital signal processing, cryptography [1], error detection and correction, and more. Here are some of the key advantages of using a Linear Feedback Shift Register: Efficient Pseudo random Sequence Generation: LFSR are adept at generating pseudo random sequences with relatively simple hardware [2]. These sequences have statistical proper- ties that resemble truly random sequences, making them useful in encryption algorithms and simulations [3]. Fast Operation: They can perform their operations (shift and feedback) very quickly, which is advantageous in applications where high-speed processing [4-6] is necessary, such as in communication systems. Error Detection and Correction: LFSRs are employed in various error detection and correction techniques [7-9], such as Cyclic Redundancy Checks (CRCs). They can efficiently identify errors in data transmission and provide a means to correct them.

Shift Register Counters: LFSRs can be configured to operate as counters. This is useful in applications requiring counting or sequencing operations.

Fig. 1 shows schematic unidirectional pulse-latch circuit 1- bit binary-code shift-register consisting of D latch [10-12]. The unidirectional contain one latch including reset signal and one pass transistor. They have consisted of 10 transistors.

Fig. 2 demonstrates the unidirectional pulse latch's oper- ation waveform. The unidirectional pulse-latch (Q and Qb) takes different data input (D and Db) when the clock signal (CL-pulse) is high.

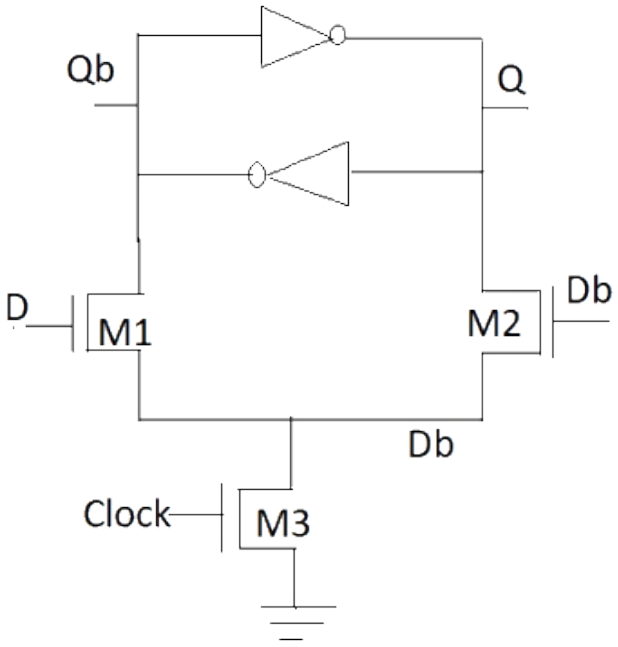

Fig. 1. Conventional Unidirectional Pulse-latch Circuit [18]

The unidirectional N-bit pulse-latch based shift register can be executed by applying the linear feedback adding with XOR gate and NOT gate in unidirectional N-pulse-latch shift register respectively [13-14]. Therefore, the pulse-latch based linear feedback shift register can lessen the delay and increase data security by exchanging XOR and NOT gate as feedback in the N-bit shift register with pulse-latch and pulse clock signals [15-18].

In short unidirectional latch based linear feedback shift reg- ister is suggested. They reduce delay and increase data security by replacing shift register with proposed unidirectional binary code-latches. This paper's remaining section is explained as follows. Describe the proposed linear feedback shift register architecture in section II. Section III is detail study comparison and various analysis and finally, in section IV, Conclusions are presented.

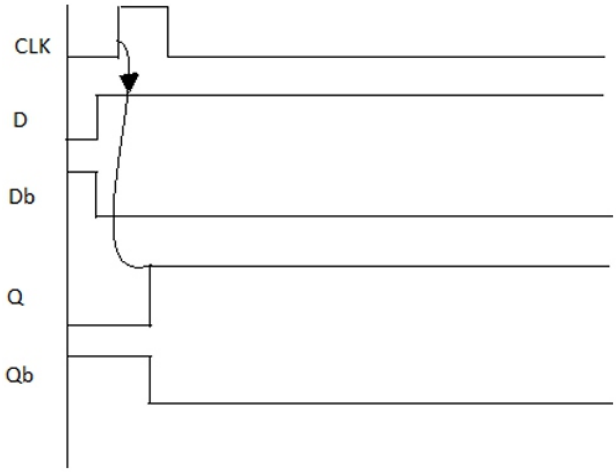

Fig. 2. Conventional Unidirectional Pulse-latch waveform [18]

II. ARCHITECTURE

A. Proposed Latch-Based Binary-Code Shift- Register

The Traditional 4-bit D latch-based binary-code shift- register is depicted in Fig.3. Initially, all data was reset by the binary-code shift-register using the reset signal. Every clock cycle, it shifts the data '1' right by one bit. The pattern of the shifting of the data recognized by the other user, very easily. In this reason the security of data will lose of latch-based shift-register.

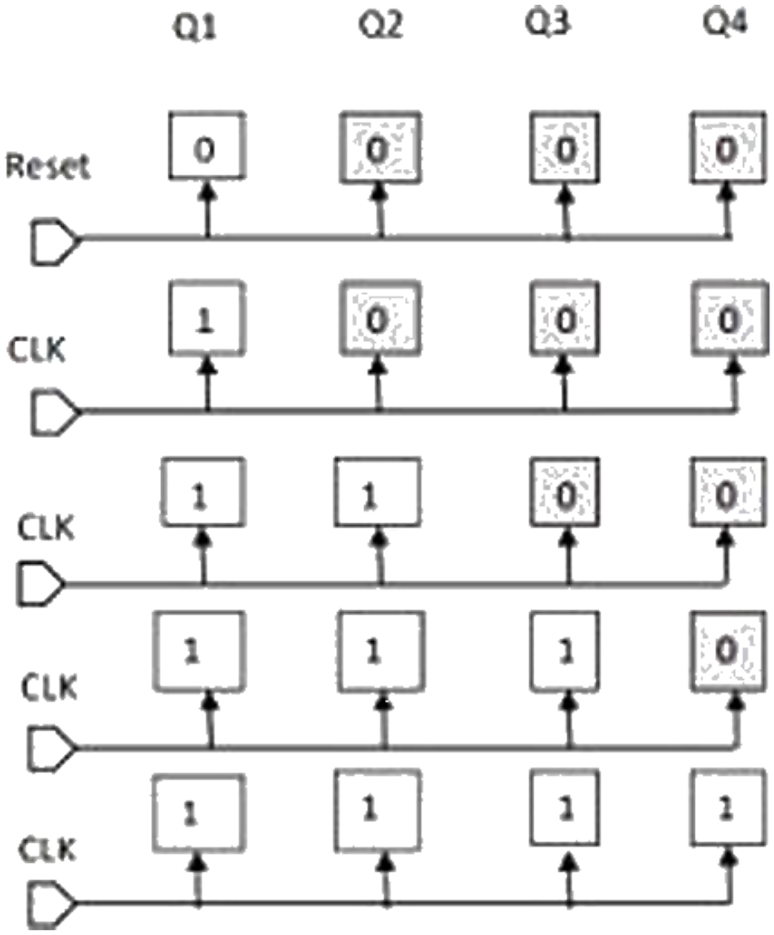

Fig. 3. Conventional unidirectional 4-bit Normal feedback-based binary-code shift-register [18]

However, the latch and two signals (CLK-odd and CLK- even) are used in the proposed linear feedback binary-code shift-register dissipated in the Fig. 4. We apply the XOR gate as feedback for improving the security purpose as per requirement. Here we adjust of the XOR gate after 4-bit latchbased shift register and all output of XOR gate attached to the first latch-based shift registers feedback as input.

Fig. 5 shows again the proposed linear feedback binary- code shift-register. Here we applying NOT gate after 4-bit latch-based shift register and combine output of NOT gate forwarding to the first latch-based shift registers feedback as input. By activating the odd and even latches, it can shift the

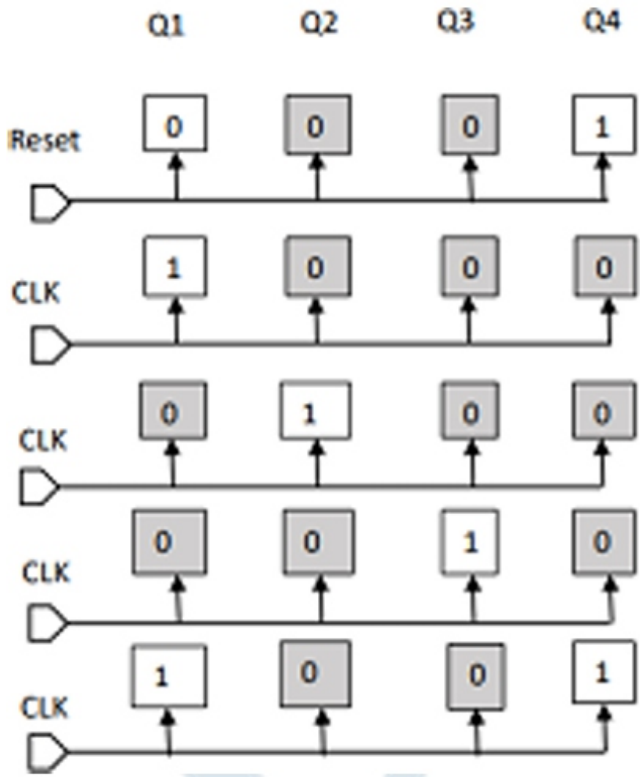

Fig. 4. Proposed unidirectional 4-bit XOR feedback based binary-code shift- register

data to ’1’. Because of generating random data as well as XOR gate, the data shifting pattern will separate then previous pattern of conventional latch-based circuit. Hence the security of the data will increase and secure from hackers.

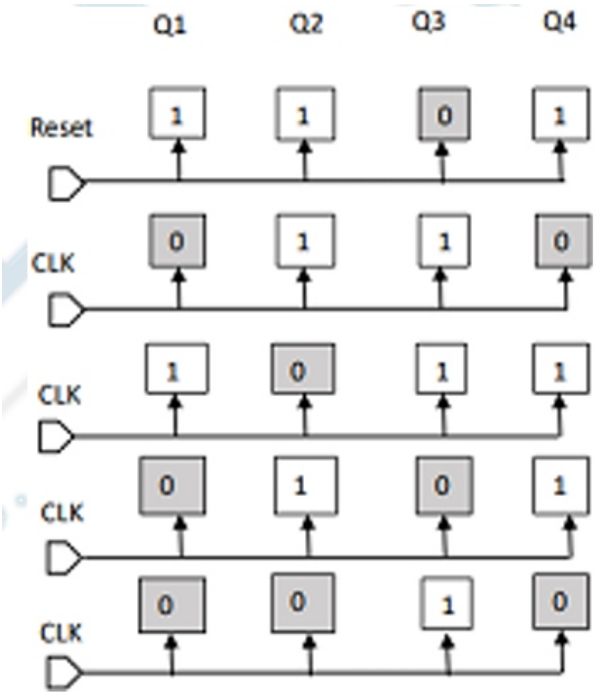

Fig. 5. Proposed unidirectional 4-bit NOT feedback based binary-code shift- register

Fig. 6 shows the conventional 16-bit binary-code shift- register that is unidirectional. It used to reset for initialize of data and CLK-signal for synchronized the data. It shifts the data '1' to right when the clock signal is CLK-odd or CLKeven and so on data will be shifted respectively. Fig. 7 shows the proposed unidirectional 16-bit binarycode shift-register. The alignment of this 16-bit shift register is that the output of the first unidirectional latch is connected to the input of the second unidirectional latch and so on. For the reset system a pin RESET connected to every unidirectional latch. The unidirectional latch which is present in odd position with connected to the CLK-odd and which unidirectional latch present in even position with connected to CLK-even. For the enhance security purpose we provided feedback as XOR and NOT gate to change the data forwarding pattern

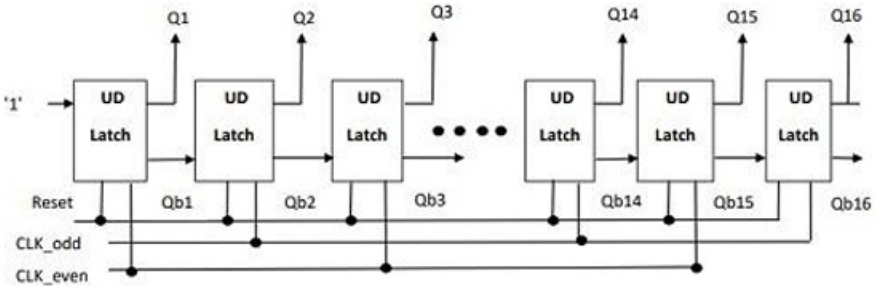

Fig. 6. Conventional unidirectional 16-bit binary-code shift-register [18]

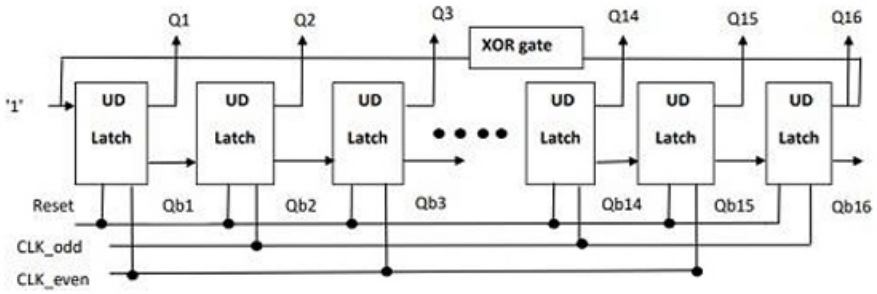

Fig. 7. Proposed unidirectional 16-bit binary-code shift-register

which is not easy to recognize by the other user and hacker. If you want more to more change the pattern of data forwarding so we have to apply more XOR and NOT after 4bit unidi- rectional latch. At the resultant the feedback of unidirectional latch is not forwarding directly to input after one XOR gate while the data forward have to more XOR gate. The performance of XOR gate is when the both bits are same like 0,0 or 1,1 so the resultant will be (Q= 0) and the both bit of alternate like 1,0 or 0,1 so the resultant will be (Q= 1). For this alternative feature of XOR gate the data of coming as feedback have been changed.

III. SIMULATION AND RESULTS

Fig. 8 shows the simulation waveform of proposed unidirec- tional binary-code shift-register, which were simulated with a 90nm CMOS process at a supply voltage of 1.8v and a clock frequency of 100MHz. The unidirectional linear feedback shift register shifts the data '1' right with CLK-odd and

CLK-even respectively, when did not apply the linear feedback of the unidirectional latch. The pattern of data shifting shown in Fig. 8 is very simple for recognized by another user. Here its advan- tage is that the power consumption is 283.80 uW and take less delay 14.39ps but this system is not secure as per simulation waveform. Table I shows that comparison among different linear shift register when apply XOR gate as feedback, NOT gate as feedback and no feedback. Approximately 94.59% less power is consumed by a NO feedback linear shift register than a NOT gate feedback linear shift register, and 95.16%

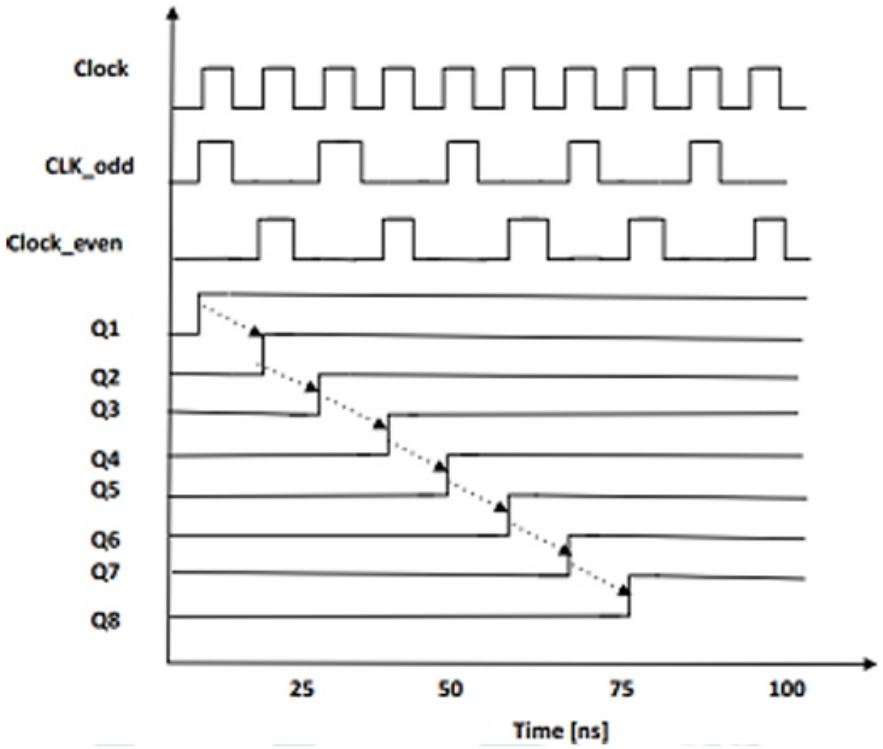

Fig. 8. Simulation waveform of Conventional binary code shift-register [18]

less power is consumed by an XOR gate linear feedback shift register. Further delay parameter by no feedback linear shirt register is approximately 86.72% less than XOR gate linear feedback shift registers and approximately 27.40% less than NOT gate linear feedback shift register. The comparison of the security is higher when we apply XOR gate as feedback in the linear shift register.

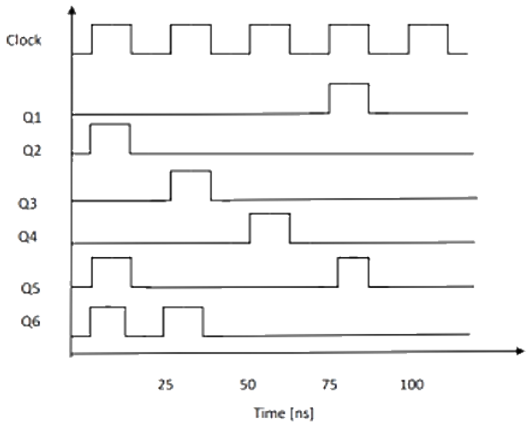

Fig. 9. Simulation waveform of proposed binary-code shift-register

Table I. Performance, Comparison, Different, Linear, Feedback

S. No.	Parameter	Normal feedback	XOR feedback	NOT feedback
01	Power [W]	283.8e-6	5.87e-3	5.25e-3
02	Delay [s]	14.39e-12	1.91e-12	380.2e-15
03	VDD (V)	1.8	1.8	1.8
04	Frequency [MHz]	100	100	100
05	Bit width of shift register	16	16	16
06	Size of Transistor [W/L]	120/90	120/90	120/90

IV. CONCLUSION

In this brief unidirectional linear feedback shift register is proposed. They are reducing power, delay and increase security by replacing XOR gate and NOT gate as feedback in linear shift register. Using a 90nm CMOS process, the proposed 16-bit linear feedback shift registers were simulated. They consume power 94.59% and 95.16% with Vdd = i.8V and a clock frequency of 100MHz. For security purpose is better XOR feedback linear shift register and for low power consumption is better is no feedback linear shift register and for less delay purpose is better NOT gate linear feedback shift register.

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