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Aims and Scope

Journal of Semiconductor Science & Technology is a journal of high quality devoted to the publication of original research papers on all aspects of semiconductor research and applications. The journal publishes original research papers on main aspects of experimental and theoretical studies of the properties of semiconductors and their interfaces. Appropriate subjects include but not limited to electrical properties, optical properties, device design, device fabrication, materials processing, materials and device analysis, process monitoring, reliability. Review articles in selected areas are published from time to time.

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Analysis of Electrical Characteristics Changes Due to Physical Parameter Variations in Dual-Gate Feedback Field Effect Transistor

Hangwook Jeong1 and Min-Woo Kwon2,

ABSTRACT

Conventional MOSFETs have reached a physical limit with a subthreshold swing of approximately 60 mV/dec at room temperature. To overcome this, various Beyond C-MOS devices are being researched, with thefeedback FET (FBFET) attracting attention due to its highly ideal subthreshold swing and high on-current. However, the FBFET operates much more sensitively compared to conventional MOSFETs. Therefore, analyzing theelectrical characteristics of the device as its physical parameters are varied is crucial in FBFET research. Despitethis importance, research and application of FBFETs have not yet made significant progress, and there is a lackof data analyzing the characteristic changes with parameter variations. In this study, we used a Dual-Gate FBFETto observe changes in electrical characteristics by varying the lengths of the gate and control gate, oxide and bodythickness, doping concentration, and the concentration and level of interface traps. An increase in the gate and Control gate lengths led to an increase in threshold voltage, and an increase in oxide thickness also resulted in a higherthreshold voltage. An increase in body thickness led to an increase in both on-current and threshold voltage, and anincrease in P− and N− doping concentrations resulted in a higher threshold voltage. Additionally, the applicationof interface traps in the gate and control gate regions increased the threshold voltage. This study's comparison andanalysis of these simulation results confirmed that parameter changes in the gate region critically impact deviceoperation more than changes in the control gate region. This finding highlights the need to pay closer attentionto parameter variations in the gate region compared to the control gate during device design and manufacturingprocesses. We expect that this analysis will significantly aid further research and application of FBFET devices.

Index terms: *Steep switching, low power, beyond C-MOS, sensitivity, control gate, dual-gate, feedback FET*

I. INTRODUCTION

Conventional MOSFETs have reached the physical limit of a subthreshold swing (SS) of 60 mV/dec [1]. Thisphysical limit of the SS value poses a significant challengein reducing the operating voltage of devices, as it leads toa substantial increase in standby power due to leakage current [2]. As the demand for high switching speed and lowpower device operation grows, various beyond CMOS devices such as T-FET, NCFET, FEFET, and feedback field effect transistor (FBFET) are being actively researched[3]. Among these, FBFET stands out due to its extremelylow SS close to 0mV/decade and high on/off ratio, making it a promising candidate for low-power operation andsteep switching behavior [4].However, FBFETs operate more sensitively comparedto conventional MOSFETs, especially the Dual-

Gate FBFET, which has more parameters and variables thanconventional MOSFETs. For instance, the Dual-GateFBFET has two gates and four different doping levels inthe body, making device analysis more complex. Additionally, the device operates with a very steep switching behavior due to its near 0mV/dec SS value, leading tohigh operational sensitivity. Therefore, a thorough analysis of the electrical characteristics resulting from changesin device parameters is crucial for the research and application of these devices. Despite this, fundamental analysesof Dual-Gate FBFET devices remain insufficient.

In this study, we analyze the impact of various parameters on the electrical characteristics of Dual-GateFBFET devices by altering each parameter and observing the resulting electrical behavior. We examine the effects of changing the gate and control gate lengths, oxideand body thicknesses, doping concentrations, and interface traps on the device's electrical characteristics. By assessing the influence of these parameter changes, we aimto identify which variations have the most critical impacton device operation. We expect that this research will significantly contribute to future studies and applications ofhighly sensitive Dual-Gate FBFET devices by providing a clear analysis of their electrical characteristics. In thispaper, for convenience, we refer to Dual-Gate FBFET asFBFET.

II. ARCHITECTURE AND MECHANISM

Fig. 1 illustrates a schematic model of the FBFET structure. Fundamentally, the device shares some similarities with conventional MOSFETs. The FBFET requires a silicon on insulator(SOI) structure to form a potential barrier and well. The silicon body is doped with N+, P−, N−,and P+ regions starting from the source area. The sourceand drain are in contact with the N+ and P+ regions, respectively, while the gate and control gate are positionedcentrally, side by side, on top of the oxide.Fig. 2 explains the operating principle of the FBFET using an energy band model. The following describes each

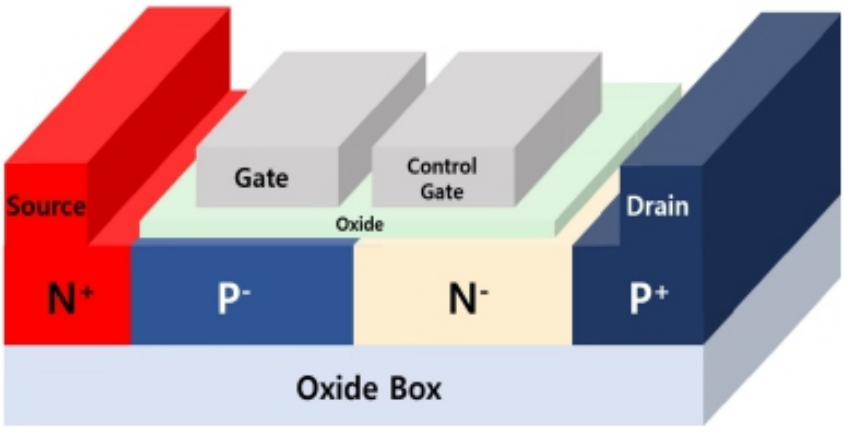

Fig. 1. FBFET structure.

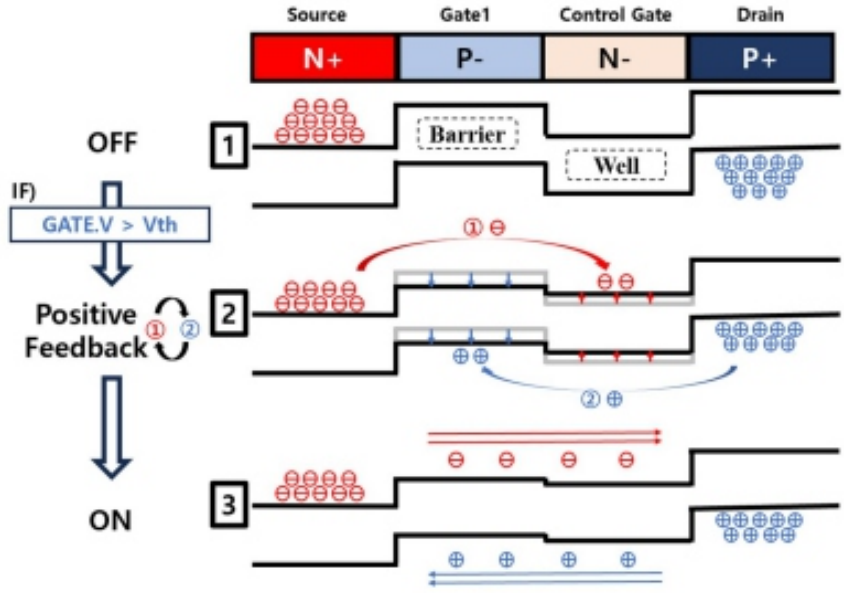

Fig. 2. FBFET operation mechanism.

step of the energy band diagram in Fig. 2.

(1) The P− region's energy band creates a potential barrier that blocks electrons from the N+ region, while the N− region forms a potential well that preventsholes from the P+ region from crossing.
(2) When a positive voltage is applied to the gate, the potential barrier lowers, allowing electrons from the N+ region to enter the potential well. Theses electronsreduce the well's depth, enabling holes from the P+region to move into the P− region. The presence ofholes lowers the barrier, allowing more electrons tocross over. This process repeats and accelerates, creating positive feedback.
(3) As the positive feedback continues, the potential barrier lowers, the well becomes shallower, and the energy band flattens. Once flattened enough, the device current flows rapidly.

Through this process, we can understand the basic operation of the FBFET. Additionally, at the pre-operation stage, as shown in Fig. 2(1), the depth of the potential wellcan be adjusted by controlling the voltage of the controlgate. A deeper potential well delays the device's operation onset, indicating that the control gate voltage can beused to adjust the device's threshold voltage [5].

III. ANALYSIS METHOD

1. Basic analysis information

The device analysis was conducted using SILVACO's T-CAD simulation. In this study, the trap analysis applied the interface trap model.

The device threshold voltage was measured using the Constant Current method. The FBFET has a SS close to 0mV, making it difficult to extract the differential value of the characteristic curve. Therefore, the Constant currentmethod is used instead of the Gm max technique. For theConstant current method, the reasonable turn-on current ofthe device is set to 10−6A. Given that the device exhibitsan extremely small SS value and a steep turn-on characteristic, minor deviations at 10−6 A can be disregarded,making the application of the Constant current method appropriate.

2. Parameter value

The analysis of the electrical characteristics in this study is based on observing the variation of drain currentwith gate voltage sweep. Here, a drain voltage of 0.8V anda control gate voltage of 2V were applied to form the potential well, while the gate voltage was swept from 2V to3V to observe the change in drain current.

Table 1 summarizes the design parameters of the deviceand doping concentrations used in the study. For comparison of the effects of gate and control gate lengths,the lengths of the gate and control gate were set to thesame 200nm. The oxide thickness was 10nm, and the bodythickness, which determines the height of the channel, was100nm. Regarding doping concentrations, P− doping wasprioritized and applied to the entire body, with the lowestdoping concentration at 1017cm−3. Subsequently, N− doping was applied at 1018cm−3, and finally, dopants were injected at a concentration of 1020cm−3for N+ and P+. Eachparameter was chosen to optimize the observation of the device's electrical characteristics and is unrelated to thesuperior performance indicators of the device.

IV. RESULTS AND DISCUSSION

The electrical characteristics of the device were measured by varying the lengths of the gate and control gate, the thicknesses of the oxide and body, and the doping concentrations, along with variations in traps.

Table 1. (a) Design parameters, (b) Doping concentrations.

(a)

Design parameters (nm)	
Gate length	200
C.Gate* length	200
Oxide thickness	10
Body thckness	100
Full length	800

(b)

Doping concentration (cm^{-3})	
N^+	1×10^{20}
P^-	1×10^{17}
N^-	1×10^{18}
P^+	1×10^{20}

1. Size variations

Fig. 3 presents a graph illustrating the electrical characteristics observed while varying the lengths of the gate and control gate. The lengths of the gate and control gate refer not only to the lengths of the contacted gate and control gate but also to the inclusion of the silicon body beneaththem. For example, doubling the gate length means thatthe silicon body beneath the gate is also doubled in size.

The lengths of the gate and control gate were varied from 200nm to 400nm at intervals of 50nm. It was observed that the threshold voltage increased with increasinglengths of both the gate and control gate. Furthermore, thevariations in characteristics due to changes in gate lengthwere more pronounced compared to changes in the control gate.

Table 2 provides a summary of the changes in threshold voltage corresponding to variations in the lengths of the gate and control gate. The rate of change in threshold voltage due to variations in gate length was significantlyhigher compared to the rate of change in threshold voltagedue to variations in control gate length.

Additionally, when comparing the total change inthreshold voltage with reference points of 200nm and400nm, the change in threshold voltage due to variationsin gate length was 0.1 V, whereas for the control gate, itwas 0.05 V. It was evident that the change in thresholdvoltage due to variations in gate length was much greater.Upon examining the rate and magnitude of threshold volt-

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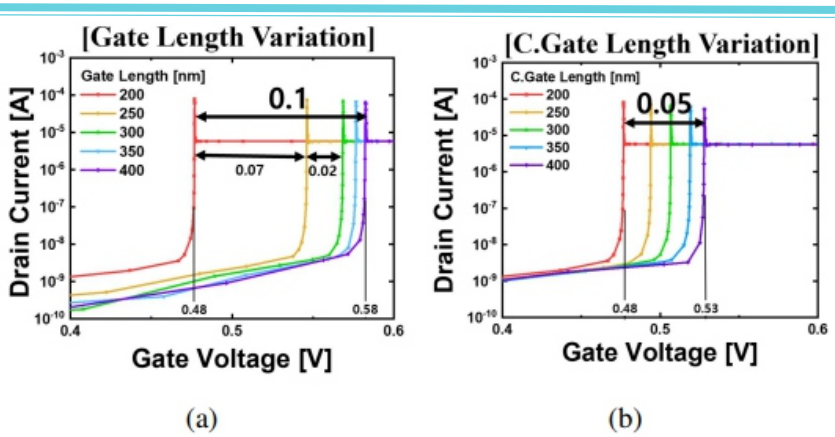


Fig. 3. IV characteristics according to (a) Gate length variations and (b) Control gate length variations. An increase in gate and control gate length leads to a rise in threshold voltage.

Table 2. Threshold voltage differences with Gate and Control gate length variations. The effect of Gate length is more dominant than that of Control gate length.

[V_{th} differences in Gate and Control gate length variation]

Length variation[nm]	200~250	-70%	250~300	-60%	300~350	-25%	350~400	200~400
Gate V_{th} difference [V]	0.07		0.02		0.008		0.006	0.1
C.GATE V_{th} difference [V]	0.017	-24%	0.013	-8%	0.012	-25%	0.009	0.05

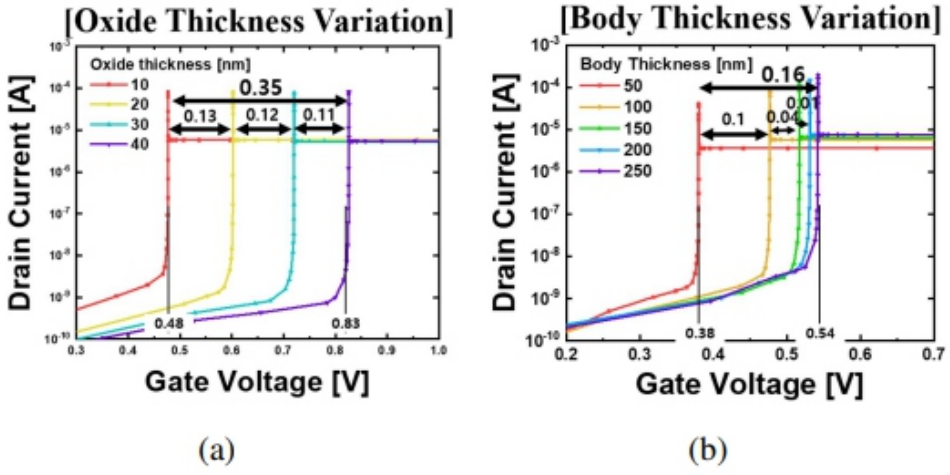


Fig. 4. IV characteristics according to (a) Oxide thickness variations and (b) Body thickness variations. An increase in oxide thickness raises the threshold voltage, while an increase in body thickness raises both the threshold voltage and the on-current.

[V_{th} differences in Oxide thickness variation]

Thickness Variation [nm]	10~20	20~30	30~40
		-7.7% →	-8.3% →
V_{th} difference[V]	0.13	0.12	0.11

[V_{th} differences in Body thickness variation]

Thickness Variation [nm]	50~100	100~150	150~200
		-60% →	-75% →
V_{th} difference [V]	0.1	0.04	0.01
On current difference [log I_d]	2.18×10^{-6}	7.39×10^{-7}	8.86×10^{-7}

age change, it was confirmed that variations in gate length had a greater impact on the electrical characteristics of the device compared to variations in control gate length.

Fig. 4(a) shows the variations in electrical characteristics of the FBFET with changes in oxide thickness. When the oxide thickness was varied from 10 nm to 40 nm atintervals of 10 nm, it was observed that the on-currentremained constant, while the threshold voltage increased with increasing thickness. This trend can be attributed tothe FBFET having a structure similar to MOSFET, andthe increase in oxide thickness leads to a decrease in thechannel control ability of the gate.

Fig. 4(b) illustrates a graph showing the variations in electrical characteristics of the FBFET with changes inbody thickness. When the body thickness was varied from50nm to 250 nm at intervals of 50nm, it was observed thatthe threshold voltage increased, and the on-current also increased.

Table 3 provides a summary of specific numerical values. The increase in threshold voltage with increasing body thickness can be understood as a result of the decrease in channel control ability due to the increase in channel height. Moreover, the increase in on-current withincreasing body thickness is attributed to the increase inchannel height, which leads to an increase in on-current.

2. Doping concentration variations

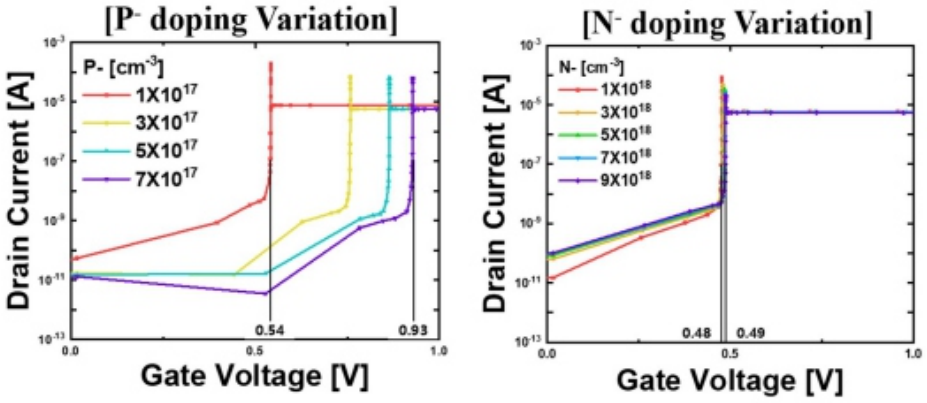
Dual-Gate FBFET operates with two gates, the gate and control gate. The doping concentrations of N+ and P+ at both ends are clear factors affecting the on-current levelafter the device turns on. Therefore, we varied only the doping concentrations of N− and P− that are considered meaningful for FBFET

doping analysis and examined the resulting graphs.

Fig. 5(a) shows the graph of the device's electrical characteristics when varying the doping concentration of P− in the body. It was observed that the on-current remainedconstant while the threshold voltage increased as the P−doping concentration varied from 1×117 cm−3to 7×1017cm−3.

Fig. 5(b) shows the graph of the device's electrical characteristics when varying the doping concentration of N− in the body. When the N− body doping concentration varied from 1×1018 cm−3to 9×1018 cm−3, the on-currentremained constant, with a slight increase in the thresholdvoltage.

Table 4 summarizes the differences in threshold voltage due to doping concentration variations. Interestingly, despite the baseline concentration of N− being higher at1?1018cm−3compared to the baseline concentration ofP− at 1?1017cm−3, the change in threshold voltage wassmaller when the N− concentration was varied by threefold, fivefold, and sevenfold. This observation suggests



(a) (b)

Table 4. Threshold voltage differences with doping concentration variations. The effect of P^- doping is more dominant than that of N^- doping.

[V_{th} differences in Doping concentration variation]

P- concentration Variation [cm^{-3}]	1×10^{17} ~3×10^{17}	3×10^{17} ~5×10^{17}	5×10^{17} ~7×10^{17}
V_{th} difference [V]	0.22	0.11	0.06
N- concentration Variation [cm^{-3}]	1×10^{18} ~3×10^{18}	3×10^{18} ~5×10^{18}	5×10^{18} ~7×10^{18}
V_{th} difference [V]	0.003	0.005	0.002

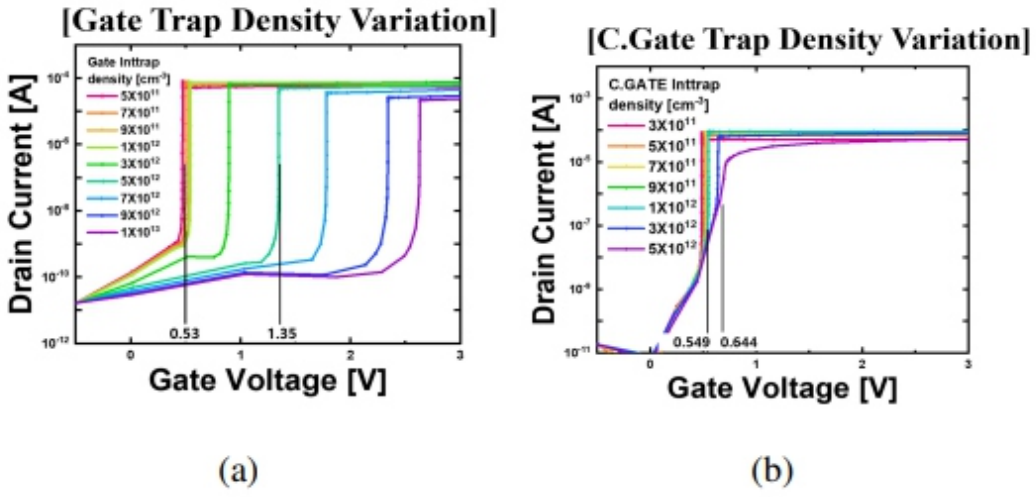
that changes in P− doping in the body have a more significant impact on the device compared to N− doping.

3. Interface trap variations

Interface traps in FBFET occur at the boundary between the silicon body and the oxide layer. We classified the application of interface traps into those applied to the gate control gate separately, as well as those applied to theentire range, and aimed to assess the influence of trap density and trap level variations on interface traps.

Fig. 6 depicts the graph of electrical characteristic variations when interface traps are applied below the gate orcontrol gate ranges, with trap density varied. In this case,the trap level is kept constant at 0.56 eV. It is observedthat regardless of the position of the gate or control gate,an increase in interface trap density leads to an increase inthreshold voltage.

Table 5 summarizes the changes in threshold voltagewithin the range of trap densities from 9 × 1011 cm−3 to 5 × 1012 cm−3, as shown in Fig. 6. It is notable that thechange in threshold voltage due to the application of gateinterface traps is significantly larger compared to that of the control gate. Additionally, Fig. 7 presents the results of



(a) (b)

Fig. 6. IV characteristics according to Trap density variations. An increase in both Gate trap and Control gate trap density leads to increase in threshold voltage.

Table 5. Threshold voltage differences with Trap density variations. The effect of Gate trap is more dominant than that of Control gate trap.

[V_{th} differences in trap density variation]

Gate trap Variation [cm^{-3}]	9×10^{11} ~1×10^{12}	1×10^{12} ~3×10^{12}	3×10^{12} ~5×10^{12}
V_{th} difference [V]	0.014	0.35	0.46
C.Gate trap Variation [cm^{-3}]	9×10^{11} ~1×10^{12}	1×10^{12} ~3×10^{12}	3×10^{12} ~5×10^{12}
V_{th} difference [V]	0.005	0.01	

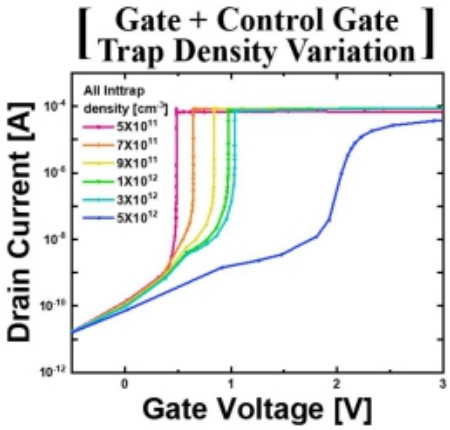
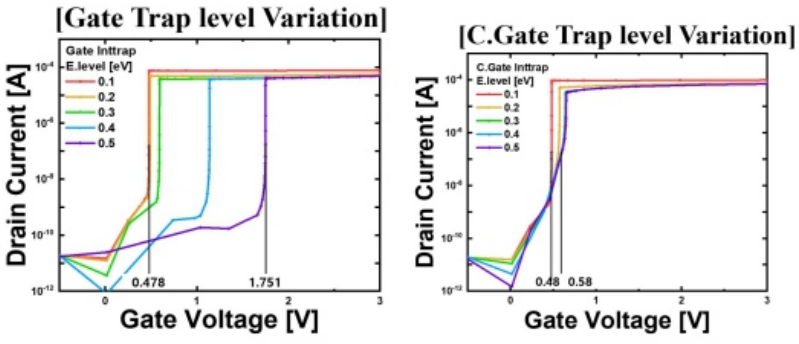


Fig. 7. IV characteristics according to Trap density across the entire range.



(a) (b)

Fig. 8. IV characteristics according to Trap level variations. An increase in both Gate trap and Control gate trap level leads to increase in threshold voltage.

observing electrical characteristic variations with interface trap density changes applied to the entire range.

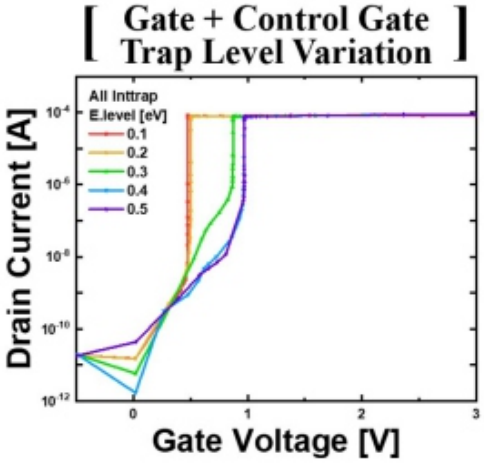
Fig. 8 illustrates the graph of electrical characteristicvariations when interface traps are applied below the gateor control gate ranges, with trap level varied. Both graphsshow that threshold voltage increases with an increase intrap level.

Table 6 summarizes the changes in threshold voltagewith variations in trap level, as depicted in Fig. 8. It isnotable that the changes in threshold voltage due to variations in gate trap level are significantly larger compared tothose resulting from variations in control gate trap level.Additionally, Fig. 9 presents the graph of observing elec-

Table 6. Threshold voltage differences with Trap level varia tions. The effect of Gate trap is more dominant tha that of Control gate trap.

[V_{th} differences in trap level variation]

Gate trap Variation [eV]	0.1 ~0.2	0.2 ~0.3	0.3 ~0.4	0.4 ~0.5
V_{th} difference [V]	0.011	0.105	0.547	0.609
C.Gate trap Variation [eV]	0.1 ~0.2	0.2 ~0.3	0.3 ~0.4	0.4 ~0.5
V_{th} difference [V]	0.09	0.07	0.001	0.003



trical characteristic variations with changes in trap level applied to the entire range.

4. Discussion

The increase in the lengths of the gate and control gate leads to an increase in channel length, resulting in an increase in threshold voltage. As the gate length increases, itdelays the accumulation of electrons in the potential wellbecause the longer channel slows down the electron transport. This is similar to the decrease in current observedin conventional MOSFETs when the channel length increases [6]. In contrast, an increase in control gate lengthleads to an extension of the potential well, requiring morecharge to raise the energy band sufficiently. Therefore, increases in both the gate and control gate lengths delay theFBFET's operation time.

An increase in oxide thickness reduces the gate's control over the channel, leading to an increase in the threshold voltage [7]. This reduced control means a higher gatevoltage is required to lower the potential barrier sufficiently, resulting in an overall increase in threshold voltage.

An increase in body thickness leads to an increase inthe on-current. Since FBFETs must maintain electrons and holes in the feedback mechanism, they are fabricated on

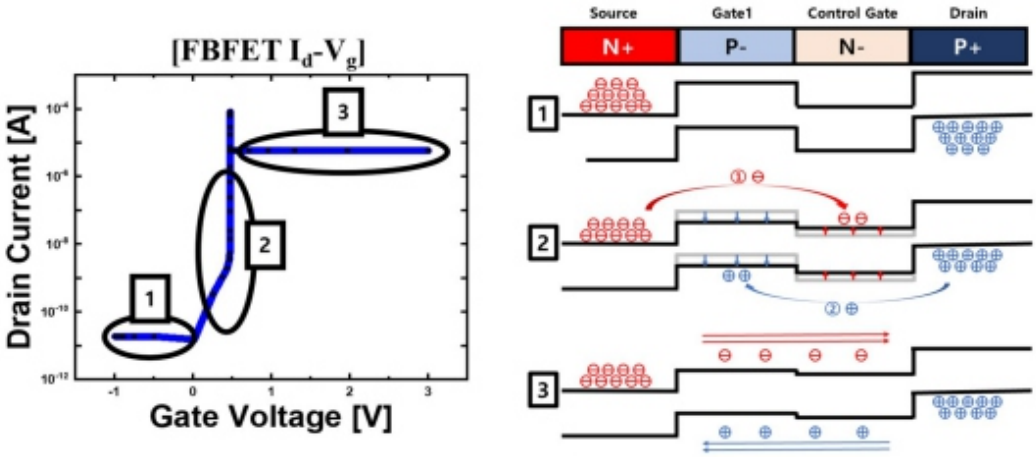


Fig. 10. IV characteristic of FBFET and energy band.

SOI wafers. Once the FBFET turns on, the entire body acts as the channel. Thus, a thicker body increases the channel height, enhancing the on-current.

An increase in doping concentration leads to an increase in threshold voltage. Specifically, an increase in P− doping concentration raises the potential barrier, thereby increasing the threshold voltage. Similarly, an increase inN− doping concentration increases the depth of the potential well, also resulting in a higher threshold voltage.

An increase in the concentration of interface traps alsoraises the threshold voltage. On the gate side, as the density and energy level of the interface traps increase, moreelectrons from the source are trapped during the feedbackmechanism, decreasing the interface potential and raisingthe energy band [8,9]. As

a result, more voltage must be applied to the gate to turn the device on. Additionally, mobility decreases due to the interface traps, causing both anincrease in threshold voltage and a reduction in on-current[10]. On the control gate side, increased interface trap density and level cause holes from the drain to be trapped during the feedback mechanism, raising the interface potential and lowering the energy band. This deepens the potential well, requiring more time to turn the device on. Therefore, the threshold voltage increases and the on-current decreases due to the interface traps.

In the variations of length, doping concentration, and trap density, it was observed that changes in parametersin the gate region led to larger variations compared tochanges in parameters in the control gate region. This phenomenon can be understood through the operational process of the FBFET.Fig. 10 shows the Id-Vg graph of the FBFET alongsidethe energy bands representing the operational principlesof the FBFET.

The operational points are categorized intothree regions. Let's closely examine region 2 (the point atwhich the device turns on). Changes in the parameters ofthe control gate alter the depth and length of the potential well, thus influencing the operational point of the device. However, it's essential to remember that the filling of freeelectrons in the potential well and the occurrence of positive feedback fundamentally result from the prior loweringof the potential barrier in the gate region. Ultimately, thedevice's operational point heavily depends on potentialbarrier in the gate region. Through this, it becomes evident how changes in gate parameters have a more pronouncedeffect on the operational point of the device compared to changes in control gate parameters.

V. CONCLUSIONS

Various steep switching devices have been researched, and among them, we examined the electrical characteristic changes of the FBFET with variations in device parameters. Through this study, we found that changes in gate parameters have a more significant impact on the thresholdvoltage characteristics of the device compared to changesin control gate parameters.

The FBFET is highly sensitive,requiring thorough analysis for both research and practical applications. This study holds significant value due to thelack of detailed analysis on the electrical characteristics ofdual-gate FBFETs with varying parameters.Additionally, the FBFET has a significant drawbackin its large hysteresis characteristics [11]. The inherent mechanism of the FBFET leads to a critical issue wherethe device does not easily turn off even under reverse biasafter turning on. So, adjusting the drain voltage is requiredto turn off the device in a logic circuit. Despite this disadvantage, the device has significant potential because itconsumes far less energy compared to conventional MOSFETs, due to its SS being close to 0 [12]. Additionally, its ability to adjust operation time by controlling the control gate

voltage is a strong advantage, making it a promising candidate for use in logic operation systems [13].

The advantages of the FBFET are clear. It exhibits avery steep switching characteristic with an SS close to0 mV/dec, enabling high-speed and low-power operation.Therefore, it is crucial to conduct focused additional analysis and follow-up research to mitigate the disadvantagesof the device while maximizing its advantages.

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Analysis of the Switching Mechanism of Hafnium Oxide Layer with Nanoporous Structure by RF Sputtering

Jongho Lim1 , Myung-Hyun , and Min-Woo Kwon,2

A B S T R A C T

As the demand for advanced memory technologies grows, the development of next-generation mem ory devices is required. One promising candidate is resistive random access memory (RRAM), which is advantageous for high-density integration in three-dimensional vertical crossbar array architectures due to its simple metal-insulator-metal structure [1]. In this study, we fabricated an RRAM device and analyzed the of the HfOx insulating layer when it possesses a nanoporous structure. The HfOx insulating layer was depositedto induce the nanoporous structure by RF sputtering. When the HfOx insulating layer has a nanoporous structure,the device exhibits a minimum current existing at a specific voltage and rectifying properties. These characteristicsresult from the migration of oxygen vacancies and the presence of oxygen ions in the pores. Depending on the applied voltage magnitude, the internal electric field created by the negatively charged oxygen ions in the pores shiftsthe voltage point of the minimum current. In addition, the Schottky-like barrier modulation induced by migration of oxygen vacancies leads to a non-linear I-V switching behavior. The resistive switching mechanism observed inthe nanoporous insulating layer plays a crucial role in enhancing the device's performance. These findings provide valuable insights into understanding the electrical characteristics of other RRAM devices with similar structures.

Index terms: RRAM, HfOx, rectifying properties, nanoporous structure, Schottky-like barrier modulation

I. INTRODUCTION

Metal-oxide-based RRAM is one of the most promising non-volatile memory devices due to its high-speed switching, next-generation non-volatile memory technologies, low power consumption, high scalability, and compatibility with complementary metal-oxide semiconductor(CMOS) technology [2,3]. The resistive switching mechanism is typically attributed to the formation and rupture ofconductive filaments within the dielectric layer, which canbe induced by applying an external voltage. This mechanism makes RRAM a promising candidate for future memory applications. Among high-k materials, hafnium oxide (HfOx) is one of the most widely used dielectric materials for the development of high-performanceRRAM devices [4]. Hafnium-based high-k dielectrics offer high dielectric constants, excellent thermal stability,and compatibility with existing semiconductor fabricationprocesses [5]. In addition, HfOx exhibits a high affinity foroxygen, which significantly facilitates the formation andmigration of oxygen vacancies (Vo), an essential aspect of the resistive

witching mechanism. These properties make HfOx a highly desirable material for enhancing the relia bility and performance of RRAM devices. Consequently,we have selected hafnium oxide as the switching layer forour RRAM device. The structure of the RRAM device isa metal-insulator-metal (MIM) structure with an insulating layer sandwiched between two metal electrodes. Manystudies have explored high-density memory structures using the simple MIM configuration of RRAM. In this cross bar array structure, the sneak path current that occurs between the memory cells will induce read-out errors in the array [6]. Therefore, the sneak path current that occurs between the cells must be suppressed. To solve the sneakpath problem, several research groups have used transistors or diodes in each memory cell [7]. However, the use of selector device in memory cells leads to some limitations. First, the selector device must match the operatingrange with the memory device [8]. Second, the addition ofa selector device results in an increase in cell size, whichis a limiting factor for the integration density of memristor systems. Therefore, the self-rectifying resistive switching memory becomes one of the most promising solutionsto overcome the sneak path current problem without re quiring an additional diode. We have derived these selfrectifying characteristics to a phenomenon that emerges by RF sputtering the switching layer. Due to the natureof the sputtering process, oxide films deposited by sputtering generally have nanoporous structures, and the existence of these pores affects the performance of the device[9-11]. In this work, we have fabricated a RRAM device inwhich the HfOx layer is sandwiched between titanium (Ti)and molybdenum disulfide (MoS2) layers and studied the effect of the nanoporous structure on resistive switchingbehavior. The resistive switching characteristics of the device have induced by RF sputtering HfOx insulating layerto form pores. The device shows self-rectifying resistiveswitching behavior with a nonlinear switching characteristics. This study will provide valuable insight into the electrical characteristics of other similar devices.

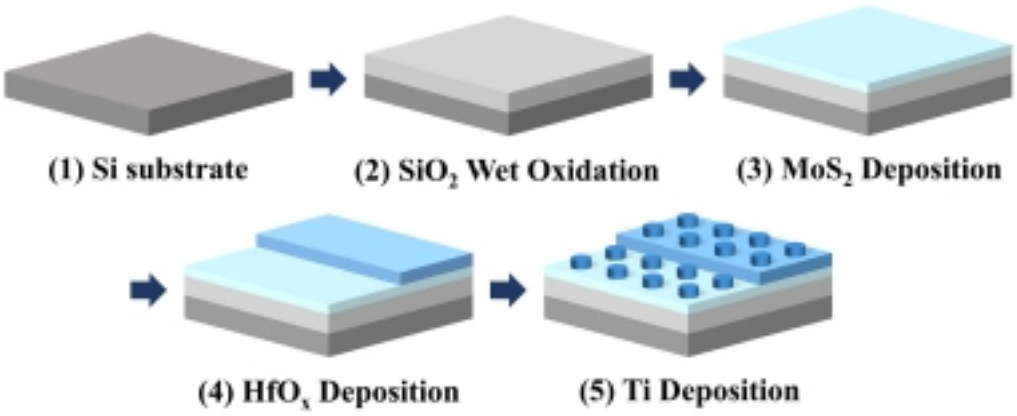
II. DEVICE FABRICATION

The fabrication process of the Ti/HfOx/MoS2 RRAM device is depicted in Fig. 1(a). The Ti/HfOx/MoS2 RRAMdevice was fabricated on a square SiO2/Si wafer substrate.Fig. 1(b) shows the schematic of the RRAM device structure. The fabrication process of the Ti/HfOx/MoS2 RRAMdevice is described in the following. First, the SiO2/Sisubstrate was rinsed with acetone, isopropyl alcohol, anddeionized water for 5 minutes for device fabrication andthen dried with N2 gas. Then, both the electrode and theswitching layer were deposited by RF sputtering. The detailed conditions of the sputtering method that used forthe fabrication of the RRAM device are summarized inTable 1. All the RF sputtering processes were carried outunder the same conditions. The MoS2 switching layer asthe bottom electrode was deposited on SiO2/Si substratefor 10 minutes. After that, to study the resistive

switching characteristics of the nanoporous structure, HfOx film was

Table 1. RF sputtering deposition conditions.

RF power	100 W
Deposition pressure	45 mTorr
Temperature	Room temperature
Ar gas flow	50 sccm



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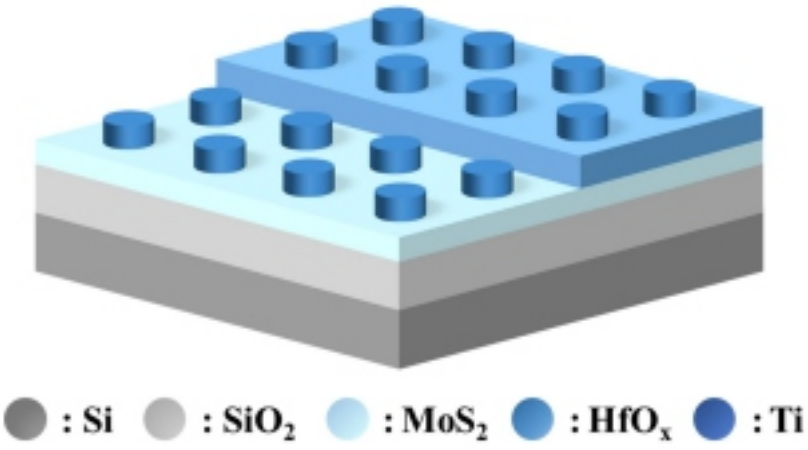


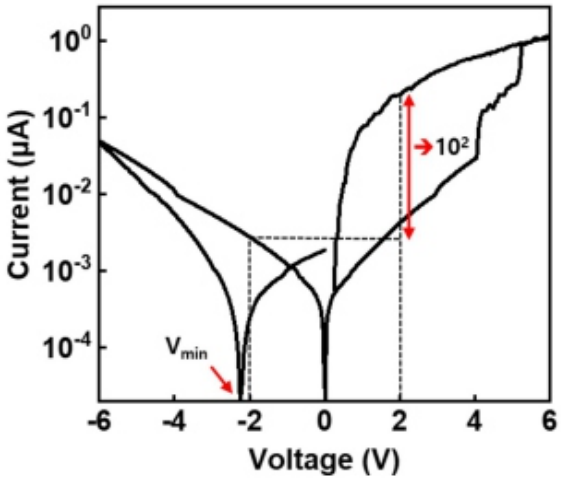
(b)

Fig. 1. (a) The fabrication process of nanoporous HfO_x based on RRAM device; (b) The proposed Ti/HfO_x/MoS_2 RRAM structure.

deposited as an insulator using a shadow mask for 20 minutes. Finally, Ti top electrode with a diameter of 400 μm was deposited through a shadow mask.

III. RESULTS AND DISCUSSION

The resistive switching characteristics of the Ti/HfOx/ MoS2 RRAM device were measured by a vacuum probestation and semiconductor parameter analyzer (AgilentB1500). The voltage bias was applied to the top electrode, while the bottom electrode was grounded. Fig. 2(a)shows the I-V characteristics of the two-terminal electrodenanoporous HfOx memory device. A positive voltagesweep was followed by a negative voltage sweep. The I-Vcurve exhibits two main characteristics. The first characteristic is self-rectifying resistive switching behavior. During forward and reverse voltage sweep, the Ti/HfOx/MoS2RRAM device exhibited a rectifying current ratio of ap proximately 102at ±2 V. This self-rectifying property canbe explained by barrier modulation due to the migration



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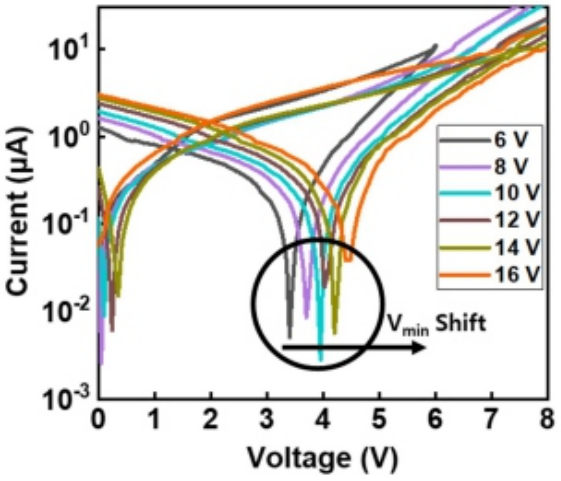

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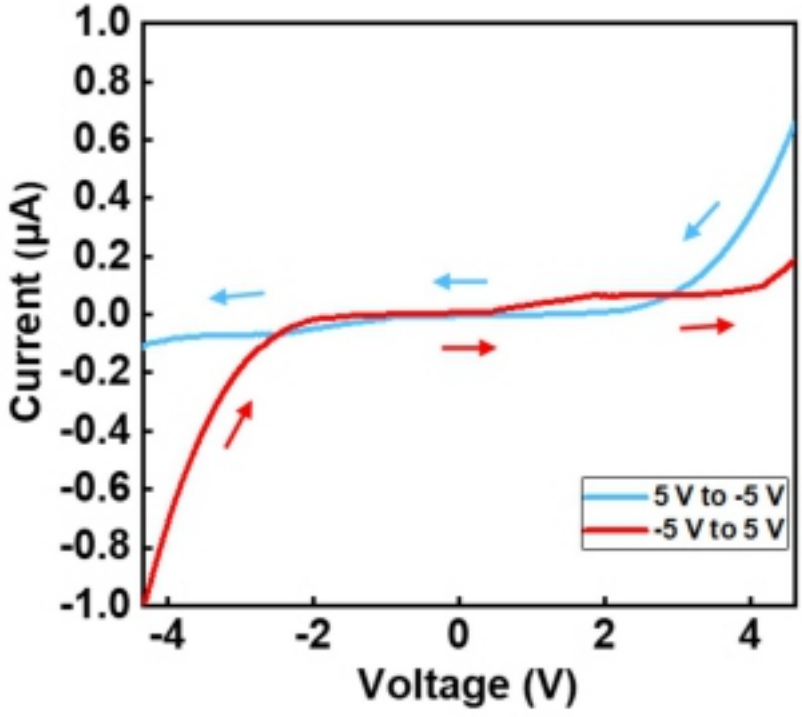

(c)

Fig. 2. (a) Representative I-V characteristics of the HfOx device; (b) Position of Vmin when supply voltage is 6 V to 16 V; (c) I-V curve for −5 V to 5 V and 5 V to −5 V voltage changes.

of Vo within the nanoporous HfOx layer [12]. The selfrectifying switching operation of the device, which exhibits minimal current flow at reverse voltage compared to positive voltage, can address the problem of sneak path current, one of the major issues in crossbar arrays [13].The second characteristic is that the voltage point of theminimum current during the reverse sweep does not return to 0 V but exists at a specific negative voltage. In thenanoporous switching layer, an internal electric field maybe formed in accordance with an external electric field inthe pores [12]. Such a characteristic enables a wide rangeof switching operations. We conducted two experimentsto demonstrate these two features (rectification characteristics and the specific voltage points of the minimum current) [14]. First, we set the applied voltage between 6 Vand 16 V to observe the relationship with Vmin (voltageposition of minimum current). Fig. 2(b) shows the changeof Vmin according to the applied voltage. As the appliedvoltage increased, a linear relationship emerged, with Vminshifting in the positive direction. This linear relationshipsupports the idea that the internal electric field created by the negatively charged oxygen ions in the pores influences the external electric field [14]. The external electric field provides

provides the necessary energy for the migration of oxygen ions within the insulating layer, causing them to move andbecome trapped in the defects or pores. Trapped oxygenions can lead to the formation of a local internal electricfield within the insulating layer. It indicates that more negatively charged oxygen ions in the pores of the switchinglayer can move as the applied voltage increases. The operation of the nanoporous RRAM device shows that the formation of the internal electric field affects the resistancestates of the device, allowing for the presence of a minimum current at a specific voltage. The results of the firstexperiment show that during the voltage sweep, the external electric field is offset by the internal electric fieldgenerated by the nanoporous HfOx layer, counterbalancing at a specific voltage point, so that the minimum current does not return to 0 V but exists at a specific voltagepoint. In the second experiment, the rectification characteristics resulting from Schottky barrier modulation due tothe migration of Vo within the insulating layer were investigated. The impact of voltage polarity on current andbarrier modulation is explained by the I-V characteristicsof the device, as illustrated by two different sweeps. Eachinitial voltage polarity was applied in both positive andnegative directions, and the current flow was observed inthe subsequent sweeps. Fig. 2© shows the blue curve representing the voltage sweep from 5 V to −5 V, while thered curve corresponds to the sweep from −5 V to 5 V.As shown in the I-V characteristics, the current response

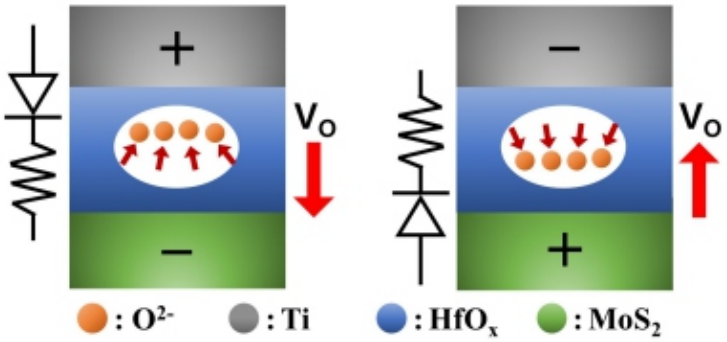

Fig. 3. Schematic cross-section of the Ti/HfO_x/MoS_2 device structure with the negative oxygen ions in the pores driven by the external electric field.

depends on the direction of the initial voltage sweep. In the 5 V to −5 V sweep (blue curve), higher current isobserved in the positive voltage region compared to thenegative voltage region. Conversely, in the −5 V to 5 Vsweep (red curve), higher current is observed in the negative voltage region. This non-linear I-V characteristic canbe attributed to the migration of Vo within the nanoporousinsulating layer, modulating the Schottky barrier at themetal-insulator interface; this corresponds to the schematics of Fig. 3 [14]. When voltage is applied, Vo within the nanoporous insulating layer begin to move according tothe polarity of the electric field. In the positive sweep (5V to −5 V), Vo are pushed towards the bottom electrodeby the initially applied positive voltage at the top electrode. The accumulation of

of Vo at one end reduces the energy barrier, forming an Ohmic-like contact and enhancing current flow in the positive voltage region. Conversely, at the opposite interface, the relative lack of Vo form aSchottky-like contact, suppressing current flow during thesubsequent negative voltage sweep (0 V to −5 V). In thereverse sweep (−5 V to 5 V), due to the polarity of theapplied voltage, Vo initially move towards the top electrode. Such movement increases the barrier height at theinterface between the bottom electrode and the insulatinglayer, forming a Schottky-like barrier, while an Ohmiclike contact is established at the opposite interface. Similarly, the barrier modulation set by the initial negative voltage suppresses current flow during the subsequent positivevoltage sweep (0 V to 5 V). The results of the second experiment demonstrate that the migration of Vo, influencedby voltage polarity, results in the formation of Ohmic-likeand Schottky-like contacts at the two interfaces of the insulating layer. The barrier modulation exhibits Schottkydiode behavior, showing non-linear I-V switching operation as the device's self-rectifying characteristic. Overall, his analysis explains the critical role of Vo migration and internal electric field generation within the nanoporousHfOx insulating layer. The linear relationship between applied voltage and the voltage point of minimum currenthighlights the dynamic nature of the internal electric field,driven by negatively charged oxygen ions. Additionally,the observed Schottky-like and Ohmic-like contacts, dependent on voltage polarity, underline the potential of thisRRAM device in mitigating sneak path currents in highdensity crossbar arrays. These insights will not only advance our understanding of the switching mechanisms innanoporous HfOx-based RRAM but also pave the wayfor the optimization and development of next-generationmemory technologies.

IV. CONCLUSION

In summary, we analyzed the characteristics that emerge when the switching layer has a nanoporous structure. The device can be fabricated at room temperature andexhibits two distinct features that set it apart from conventional memory devices. Firstly, the position of Vmin varieswith the applied voltage, which was demonstrated to bedue to the internal electric field created by the migration ofnegatively charged oxygen ions within the pores. The linear relationship observed between the applied voltage andVmin indicates a broad range of switching characteristicsthat can be achieved across a range of operating voltages.Secondly, the self-rectifying resistive switching behavioris shown to be due to Schottky-like barrier modulationinfluenced by the initial polarity of the applied voltage. This self-rectifying property has the potential to suppress sneak path currents from unselected cells in 3D verticalcrossbar array structures. This analysis demonstrates thatnanoporous hafnium-based memory devices offer significant advantages compared to non-porous oxide-basedmemory devices. The results of this study not only enhance the understanding of the switching mechanisms ofthese devices but also pave the way for the development of more efficient and reliable memory technologies.

ACKNOWLEDGMENTS

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A Second-order Delta-sigma Modulator for Battery Management System DC Measurement

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A B S T R A C T

This paper presents a second-order modified feed-forward (FF) delta-sigma modulator for battery management system DC measurement. The proposed ADC employs a modified 3-bit feedback digital-to-analog converter (DAC) with the data weight averaging (DWA) technique to improve the capacitance matching. The modified 3-bit DAC reduces the logic complexity of the DWA by simplifying the switching network of unit capacitors.Additionally, the proposed ADC adopts capacitor swapping technique between the input and reference samplingcapacitors to minimize its gain error. To further improve the performance of the proposed ADC, system-level lowfrequency chopping (CHL) and correlated double sampling (CDS) are employed to mitigate offset and flicker noise.The prototype ADC is fabricated in a 180 nm CMOS process, and the core area is 0.53 mm2. It consumes 9.48 µWfrom a 1.8 V supply voltage at an operating clock frequency of 19.2 kHz with an oversampling ratio (OSR) of 256.It achieves a dynamic range (DR) of 102.4 dB, a resolution of 7 µVrms, and an offset of 6.86 µV, resulting in aSchreier figure-of-merit (FoM) of 165.3 dB.

Index terms: *Analog-to-digital converter (ADC), delta-sigma modulator, data weight averaging (DWA), digital-toanalog converter (DAC), feed-forward (FF*

I. INTRODUCTION

In a battery management system (BMS), a voltage sensing integrated circuit (IC) is an essential block for monitoring the state of charge (SOC), which indicates the remaining power of the battery cells [1-4]. Fig. 1 illustrates the block diagram of the voltage sensing IC for BMS,which consists of a high voltage multiplexer (HVMUX) toselect battery cells, a level shifter to scale down the highvoltage of the battery cells, a voltage reference generator, and an analog-to-digital converter (ADC) [1]. Amongthese, the key building block is the ADC which requires

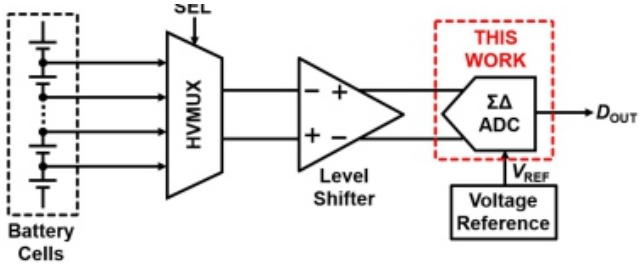

Fig. 1. Block diagram of the voltage sensing IC for BMS.

high-resolution, and delta-sigma ADCs are well suited for the voltage sensing because they can achieve high accuracy through oversampling and noise shaping [5,6].In the delta-sigma ADCs, an input feed-forward (FF) topology is widely used for high-resolution because iteases the design requirements of the integrators by processing the quantization noise only [7]. This allows forthe reduction of quantization noise and the swing range ofthe integrators by employing a multi-bit digital-to-analogconverter (DAC), and the DWA is used to correct the mis-match of unit capacitors in the DAC [8]. However, due to signal attenuation within the internal FF path, the comparator accuracy requirements become more challenging,and the load capacitance of the first integrator is affectedby the quantizer, reducing power efficiency. Given theseconstraints, the modified FF topology [9,10], which removes the internal FF path, has emerged. The load capacitance of the first integrator is no longer affected by thequantizer, and simplified passive summing reduces signalattenuation.

In addition to the power efficient topology described above, the proposed architecture employs a modified 3-bit feedback DAC with data weight averaging (DWA).The modified DAC reduces the complexity of the DWAlogic, thereby increasing power and area efficeincy. Theproposed modulator is fabricated in a 180 nm CMOS process, and achieves a dynamic range (DR) of 102.4 dB anda Schreier figure-of-merit (FoM) of 165.3 dB.The rest of this article is organized as follows: SectionII explains the architecture of the proposed delta-sigmamodulator. Section III discusses the details of the circuitimplementation. The measurement results of the prototypemodulator are presented in Section IV, and this article concludes with Section V.

II. PROPOSED ARCHITECTURE

The architecture of the proposed delta-sigma modulator is shown in Fig. 2. The modulator employs the modified FF topology and consists of a first integrator, a second integrator with an analog signal processing block, HA(z),a 3-bit flash quantizer with a passive switched capacitor(SC) adder, and a feedback DAC with DWA. The outputof the modulator, DO(z), and the outputs of two integrators, V1(z) and V2(z), are given by

$$D_O(z) = U(z) \cdot STF(z) + Q(z) \cdot NTF(z), \quad (1)$$

$$V_1(z) = Q(z) \cdot z^{-\frac{1}{2}} \cdot (1 - z^{-1}), \quad (2)$$

$$V_2(z) = Q(z) \cdot z^{-1} \cdot (2 - z^{-1}), \quad (3)$$

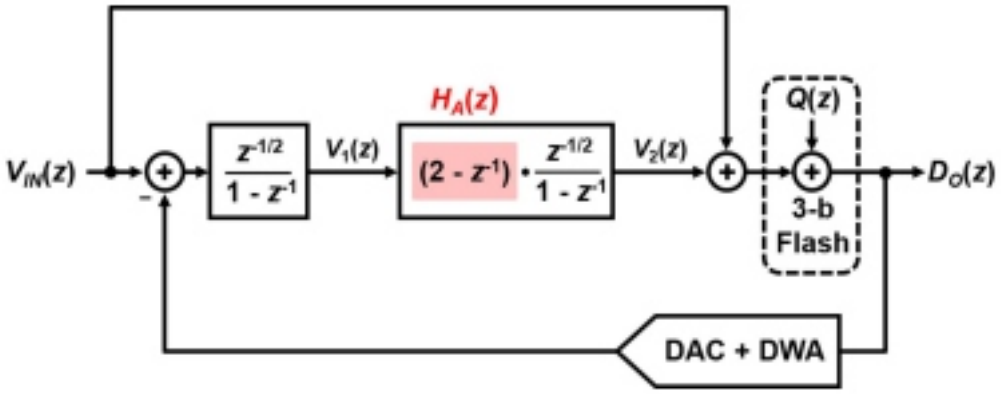

Fig. 2. Architecture of the proposed delta-sigma modulator.

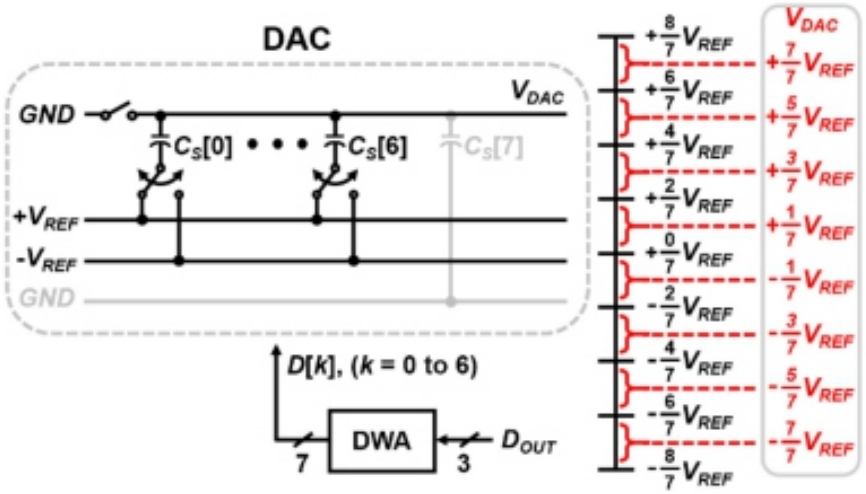

Fig. 3. The modified DAC with DWA and the output levels.

where VIN(z) and Q(z) indicate the input of the modulator and quantization noise, respectively. Thanks to the modified FF topology, integrators handle only quantizationnoise as shown in (2) and (3), which reduces the swingrange of the integrators [9,10]. Also, due to HA(z) in themodified FF architecture, the design requirement of thecomparators is relaxed, and power efficiency is increased.

For the feedback DAC, the proposed ADC adopts amodified 3-bit DAC with seven unit capacitors, removingone capacitor connected to ground, as shown in Fig. 3. Inthe modified DAC, all of the bottom plates of the capacitors switch only between +VREF and −VREF , which simplifies the DWA logic complexity. The DAC output rangesfrom −7/7VREF to +7/7VREF in steps of 2/7VREF . To reduce the mismatch between unit capacitors, the conventional DWA technique is applied [8].

III. CIRCUIT IMPLEMENTATION

1. Proposed Delta-Sigma Modulator

The overall schematic of the proposed delta-sigma modulator and its timing are shown in Fig. 4. The modulator is implemented in a fully differential structure andoperates with two non-overlapping clocks, φ1 and φ2. Inthe first integrator, DWA is employed to minimize the capacitance mismatch, and its operation is as follows. In theφ1 phase, the flash quantizer determines the 3-bit digital output, and in the φ2 phase, the reference sampling capacitors are shifted according to the output code. Two additional clock signals φ3 and φ4 are employed to implementthe transfer function 2−z−1of the second integrator. Using the thermal noise analysis presented in [11], thesampling capacitance values for both integrators were determined. To reduce the degradation of modulator performance due to thermal noise, the total sampling capac

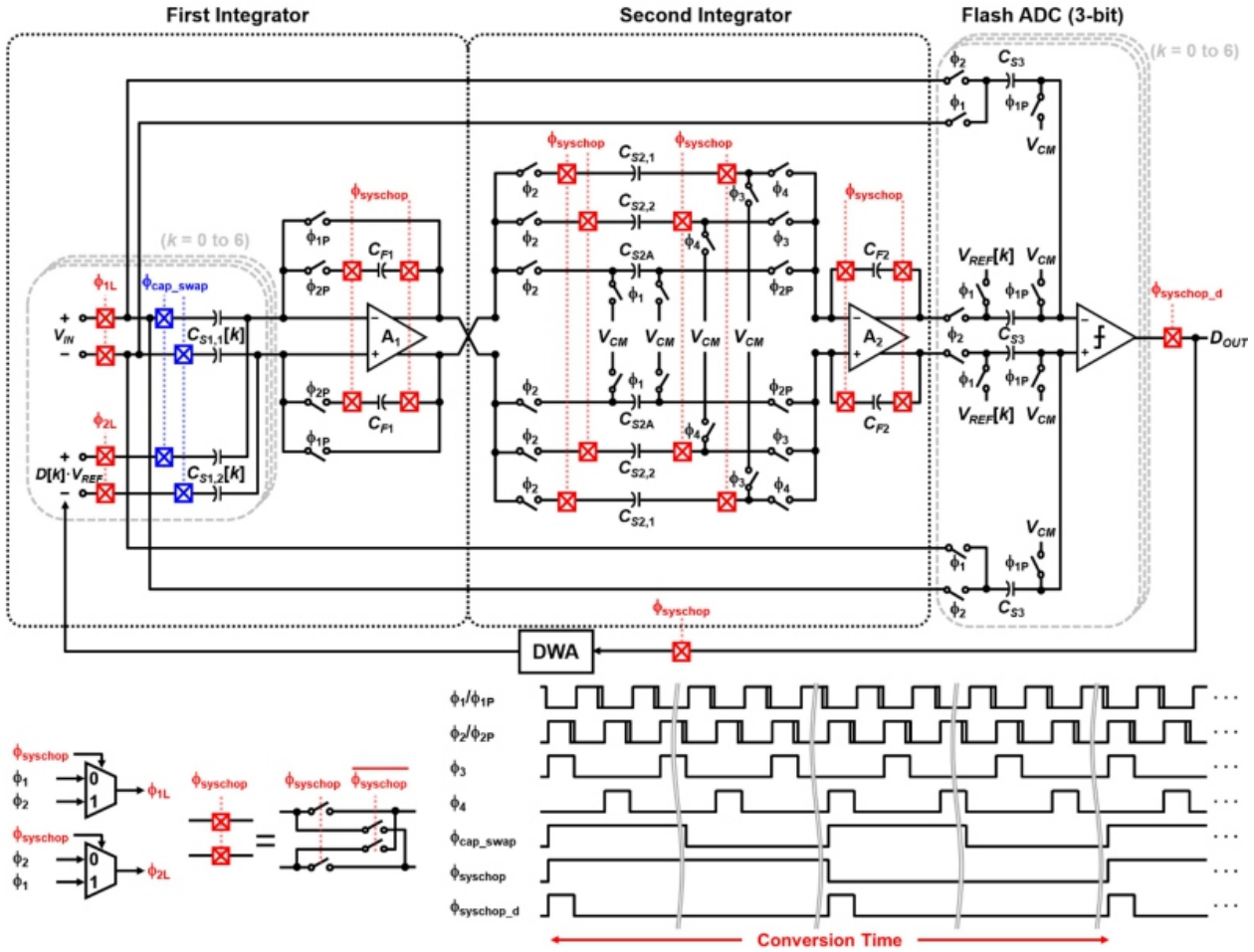

Fig. 4. The overall schematic of the proposed second-order modified FF delta-sigma modulator and its timing.

tance of the first integrator is set to be 1.5 pF, that of the second integrator to 200 fF, and the input capacitance ofthe quantizer to 100 fF, since the thermal noise generatedin the second integrator and the quantizer is shaped, allowing for smaller capacitor values [11].

A resistive-ladder (R-ladder) has been used on-chipto generate the reference voltage for the flash quantizer.Since static current is produced in the R-ladder, increasing the total resistance reduces power

consumption. However, feedthrough caused by the input stage capacitance between the quantizer's input and the reference voltageleads to distortion in the ADC [12]. To address this, themaximum feedthrough at the midpoint of the R-ladder islimited to 0.1 LSB. The total resistance is determined by the following equation

$$R = \frac{4\phi}{\pi 2^n f_{in} C}, \tag{4}$$

where φ is the feedthrough in LSB and n is the resolution of the quantizer and C is the total capacitance from the Rladder, and fin is the input frequency of the quantizer [12]. As a result, the total resistance must be set below 1.18MΩ. Considering feedthrough and static current, a totalresistance of 0.93 MΩ was chosen. This R-ladder occupies an area of 0.07 mm2.

Correlated double sampling (CDS) is employed in the first integrator to mitigate offset and flicker noise[13]. Furthermore, A system-level low-frequency chopping (CHL) technique suppresses the residual offset ofthe modulator by periodically inverting the polarity ofthe input and output [14]. Therefore, chopped switchesare employed at the input and output paths. In this design, the chopped switch control clock, φsyschop, is usedto enable one CHL transition in one conversion cycle.To match the polarity of the integration path between before and after the CHL transition, chopped switches employed for the feedback capacitors. Additionally, thechopped switches are also employed in the sampling capacitors of the second integrator, except for the additional sampling capacitor, CS2A, which is reset in the φ1 phase.During the first reference sampling after the CHL transition, since the modulator output which provides feedback to the DAC has the same polarity as the previousstate, a φsyschop_d clock signal is used to invert the outputpolarity of the feedback path to match the polarity of the input and feedback DAC [15]. This process modulates thesystematic offset and removes it after passing through thedecimation filter.

2. Loop Filter

The schematic of the first integrator and its timing are shown in Fig. 5. Bootstrapped switches are em ployed to enhance input sampling linearity [16]. To reduceADC gain error caused by the capacitance mismatch between the input sampling capacitor CS1,1[k] and the reference sampling capacitor CS1,2[k], a capacitor swappingtechnique is employed to average out the capacitancemismatch as follows: During one conversion cycle, theCS1,1[k] and CS1,2[k] arrays are swapped twice to ensurethat the averaged capacitance is used for both input andreference sampling. The schematic of the second integrator with the transfer function, $2 - z^{-1}$, and its timing are shown in Fig. 6. For the second

integrator, three sampling capacitors are employed: two sampling capacitors CS2,1,CS2,2, and an additional capacitor CS2A. During the following φ3 phase, CS2,2 and CS2A are connected to integrate theoutput of the first integratorV1[n−1] without delay. At thistime, the remainingCS2,1 samples the output of the first integrator. Then, during the subsequent φ1 phase, CS2A is re

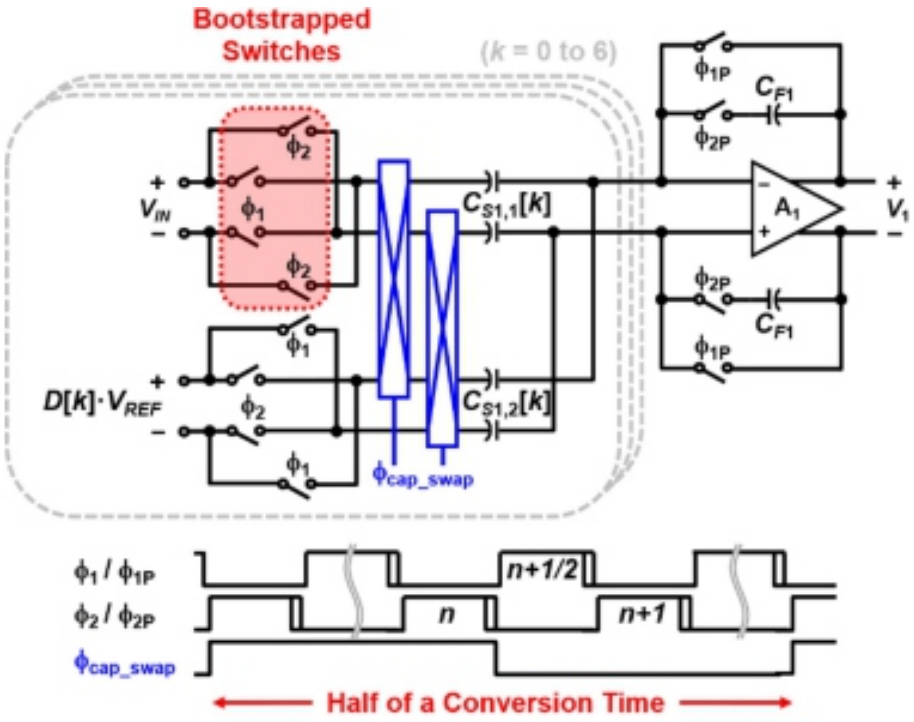

Fig. 5. Schematic of the first integrator and its timing.

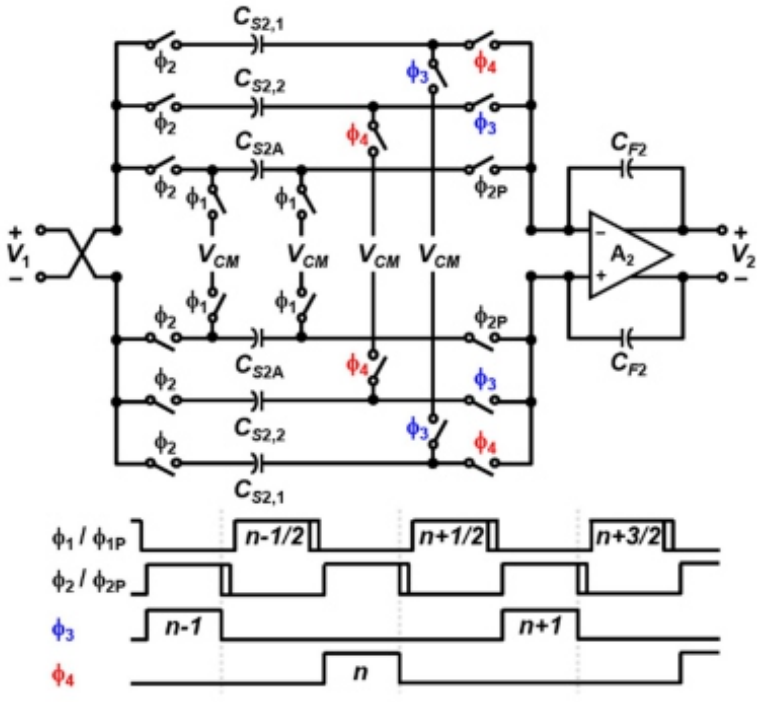

Fig. 6. Schematic of the second integrator and its timing.

set. In the following φ4 phase, similar to the φ3 phase, the previously sampled CS2,1 and CS2A are connected for integration. Finally, the output of the second integrator V2[n]becomes 2 ·V1[n]−V1[n−1], and this sequence of operations implements the transfer function 2−z−1.

IV. MEASUREMENT RESULTS

The prototype delta-sigma modulator is implemented in a 180 nm CMOS process. Fig. 7 shows the die micrographof the proposed modulator. The core area is 0.53 mm2. Fig.8 shows the power breakdown of the proposed modulator.From a 1.8 V supply, the modulator consumes 9.48 µW at19.2 kHz sampling frequency. Fig. 9 shows the measuredoutput spectrum of the proposed modulator with a 0.6 VDC input and input shorted, respectively. The measured DR is 102.4 dB and Fig. 10 shows the measured offset

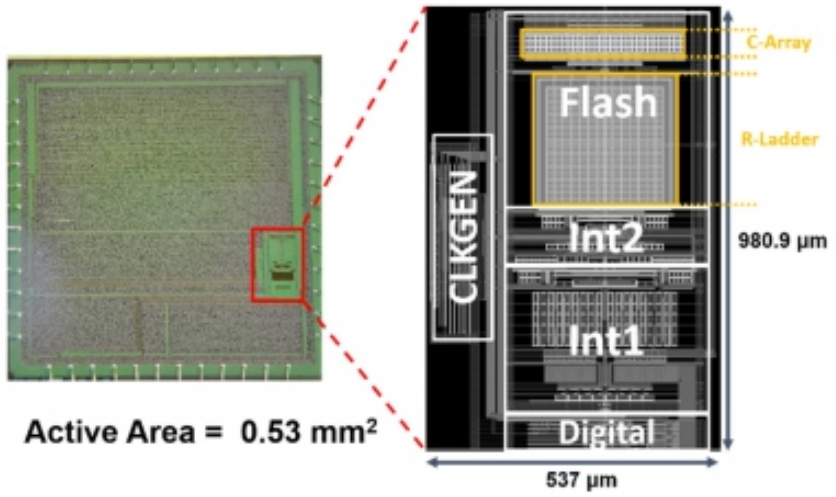

Fig. 7. Die micrograph of the proposed modulator.

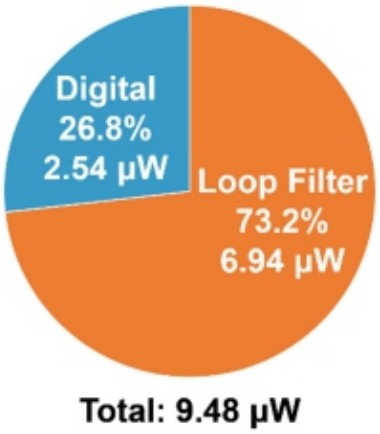

Fig. 8. Power breakdown of the proposed modulator.

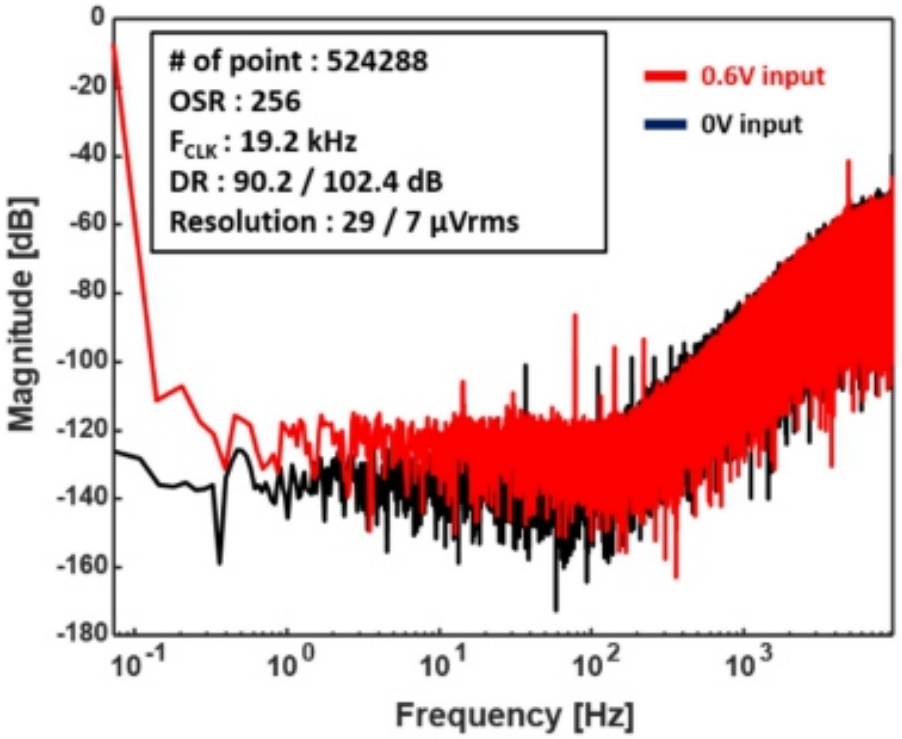

Fig. 9. Measured output spectrum of the proposed modulator.

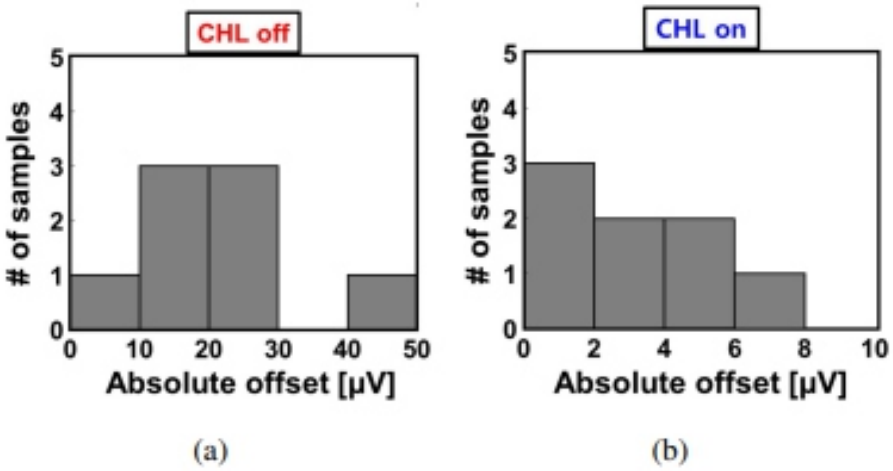

Fig. 10. Measured offset of the proposed modulator with (a) chopped off, and (b) chopped on.

with and without CHL, and for this measurement, a sinc3 filter is implemented off-chip for decimation in MATLAB.The maximum offset from eight samples without CHL is50 µV, and it drops below 6.86 µV with CHL. The measured performance of the proposed modulator is summarized and compared in Table 1.

Table 1. Performance summary and comparison table.

	This work	[17]	[18]	[19]	[20]
Architecture	DT DSM	CT DSM	CT DSM	DT IDSM	DT DSM
Process (nm)	180	65	180	180	110
F_{CLS} (kHz)	19.2	0.512	64	5000	512
OSR	256	256	128	250	128
BW (Hz)	18.75	1	250	10000	2000
Supply (V)	1.8	1.2	1.8	1.8	1.5
Power (μW)	9.48	15	2.16	83	62.43
DR (dB)	102.4	105	81.4	89.1	96.3
Resolution (μV_{rms})	7	4	-	19	-
Offset (μV)	6.86	-	-	-	-
Area (mm^2)	0.523	9.07	0.29	0.35	0.165
*FoM_s	165	153	162	162	171

*$FoM_s = DR + 10 \cdot \log_{10}(BW/Power)$

V. CONCLUSION

This paper presents a second-order modified FF deltasigma modulator for BMS DC measurement. The proposed modulator employs the modified 3-bit feedback DAC to reduce the complexity of the DWA logic, and a capacitor swapping technique is adopted to minimizethe gain error from sampling capacitance mismatch. Additionally, the CDS and CHL techniques are applied to minimize offset and flicker noise. The prototype modulator,fabricated in a 180 nm CMOS process, achieved a DR of102.4 dB, a resolution of 7 μVrms, and an offset of 6.86μV while consuming 9.48 μW.

ACKNOWLEDGMENTS

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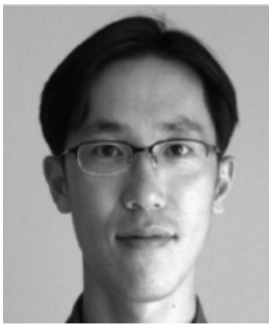

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Design Optimization of L-Shaped Gate Negative Capacitance Si/Ge Heterojunction TFET With Channel Doping

Xinfeng Zheng, Weifeng Lü, Yubin Wang, Shuaiwei Zhao, and Honglei Huo

A B S T R A C T

In this paper, to improve the performance of L-shaped gate heterojunction tunneling field-effect transistor (LG-HJ-TFET), an L-shaped gate negative capacitance Si/Ge heterojunction TFET with channel doping (NCHJCD-LTFET) was proposed, whose electrical characteristics were investigated through technology computer-aideddesign simulations in Sentaurus. The NCHJ-CD-LTFET has doping (n+-doping for an n-type TFET) in the cornerregion of the channel, which plays an important role in modulating the energy bands that reduce the bandgap between the source and channel in the doping area. Thus, compared with the LG-HJ-TFET, the band-to-band tunnelingof NCHJ-CD-LTFET occurs at a lower gate voltage (VGS), and the threshold voltage (VTH) is significantly reducedfrom 0.221 to 0.181 V. In addition, a ferroelectric layer was deposited above the horizontal gate dielectric to furtherimprove the electrical characteristics owing to the negative-capacitance effects. With comprehensive adjustment thedoping concentration of the channel corner region (NCH,CO) and the thickness of the ferroelectric layer (TFE), theNCHJ-CD-LTFET had a low VTH of 0.145 V, a high on-state current (ION) of 27.5 μA/μm, a high switching currentratio (ION/IOFF) of 2.1×108and a steep average subthreshold slope (SSAVE) of 24.92 mV/decade.

Index terms: *Band-to-band tunneling, L-shaped gate TFET, negative capacitance, channel doping, energy band modulation*

I. INTRODUCTION

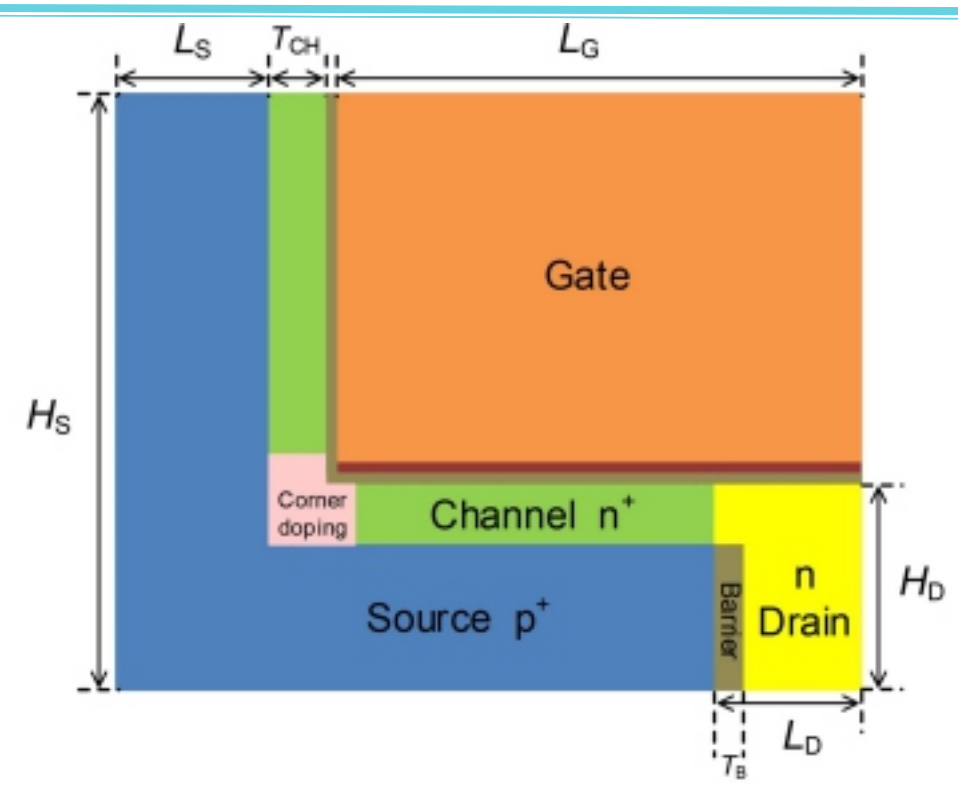
With the development of integrated circuits, the number of transistors on a chip and the operating frequency are increasing. Although these improve the chip performance, they also increase the power consumption [1]. Because complementary metal-oxide-semiconductor devicesrely on thermal injection as the carrier emission mechanism, their subthreshold slope (SS) cannot be lower than60 mV/decade at room temperature, owing to Boltzmann'styranny [2], resulting in a transistor that does not satisfy both the high-performance and low-power consumption requirements. Fortunately, tunneling field-effect trsistors (TFETs) that utilize quantum-mechanical bandto-band tunneling (BTBT) can overcome Boltzmann's tyranny and obtain sub-60 mV/decade SSs [3-9]. However, conventional TFETs have drawbacks, such as their low on-state currents (ION) [10,11]. In many proposed TFETs structures, such as L-TFETs [12,13], U-TFETs [14], and Z-TFETs [15], ION is increased by increasing the BTBT area. In particular, the performance of L-shaped channel TFETs has

been improved via doping or the addition of ferroelectric layers [16-19]. Doping engineering can achieve abrupt switching by mitigating the BTBT at the corner edge of the source region in a negative capacitance TFET (NCTFET) [18]. Recently, an L-shaped gate InGaAs/GaAsSb heterojunction TFET was presentedthat extends the source to increase the BTBT area between source and channel for increasing ION [20]. However, few studies have focused on capacitance Si/Ge heterojunction tunneling field-effect transistor with channel doping (NCHJ-CD-LTFET) wasdeveloped and investigated via technology computeraided design (TCAD) simulations with calibrated modelparameters [21]. Compared with the LG-HJ-TFET, theNCHJ-CD-LTFET has a far lower threshold voltage (VTH).The energy bands of the corner doping region are modulated via channel doping, which reduces the tunneling barrier between the source and the channel and theferroelectric layer can amplify the internal gate voltageto increase the electric potential of the channel surface.Meanwhile, the negative-capacitance effects can suppressBTBT at VGS = 0 V and reduce the off-state current (IOFF).The doping concentration of the channel corner region(NCH,CO) and the ferroelectric-layer thickness (TFE) canbe adjusted to optimize the electrical performance of thedevice, lowing power consumption and improving drive capability.

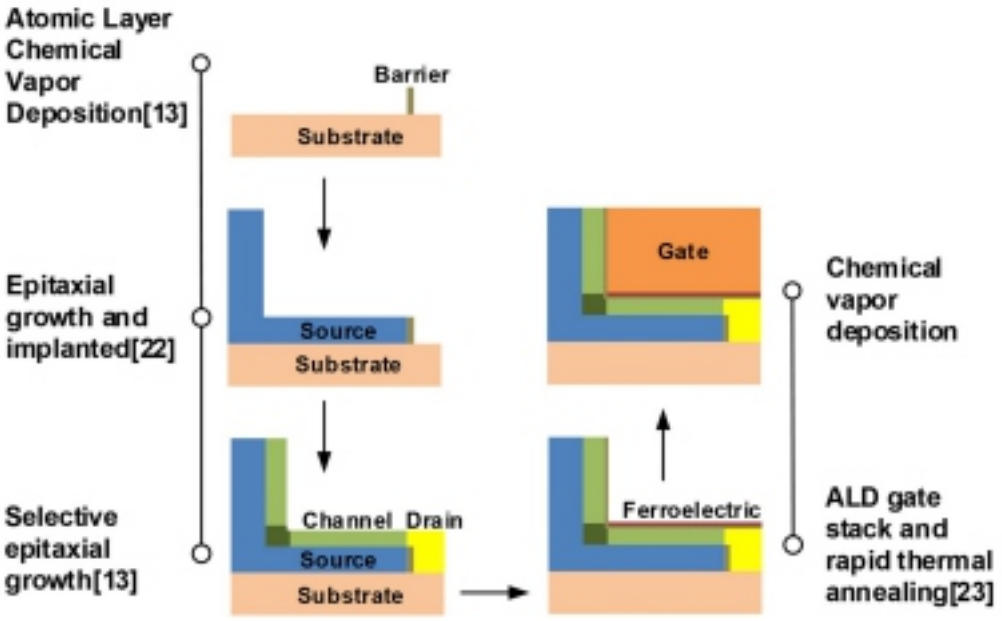
II. STRUCTURE AND MECHANISM OF THE NCHJ-CD-LTFET

Fig. 1(a) shows a schematic of the proposed NCHJ-CDLTFET structure. The tunneling junction consists of a p+ Ge source and an n+ Si channel. The drain is a silicon material, and the doping concentration of the source, drainand channel are 2 × 1019, 1 × 1017 and 1 × 1018 cm−3,respectively. The source and drain are separated by a 4-nm-thick HfO2 barrier layer. The gate dielectric is a 1-nm-thick HfO2 layer with a dielectric constant of 22. Aferroelectric layer is deposited above the horizontal gatedielectric. In addition, the work function of the gate is 4.2eV and the structural parameters are presented in Table 1.Fig. 1(b) shows the brief process flow for the fabricationof NCHJ-CD-LTFET.

Fig. 2 presents the electrostatic potential of the corner doping region. As shown, the electrostatic potential alongthe diagonal direction decreases faster than the vertical and horizontal potentials, and at the same distance fromthe gate, the diagonal electrostatic potential is lower thanthe vertical and horizontal potentials. Therefore, the energy bands can be modulated via heavy doping in this region. Figs. 3(a) and 3(b) present the energy bands with andwithout heavy doping, respectively. As shown, with heavydoping in the corner-doping region, the energy bands benddownward, and the bandgap between the source and doping region is reduced. Therefore, BTBT can occur at lowergate voltages (VGS).



(a)



(b)

Fig. 1. (a) Structure of the proposed NCHJ-CD-LTFET. (b) The brief process flow for the NCHJ-CD-LTFE.

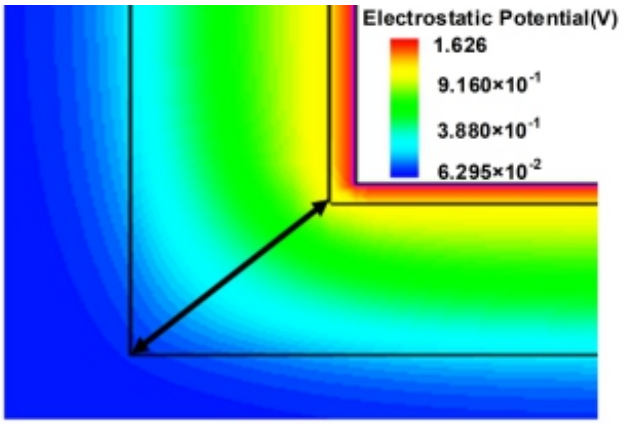


Fig. 2. Electrostatic potential of the corner doping region.

To accurately analyze the electrical characteristics of the NCHJ-CD-LTFET, the nonlocal BTBT and LandauKhalatnikov (L-K) models were used. The Kane modelparameters were F0 = 1 V/m, P = 2.5, ASi = 4.0 × 1014cm−3·s−1, BSi = 9.9 × 106 V·cm−1[24], and the L-Kmodel parameters were α = −1.299 × 1011 cm/F, β =

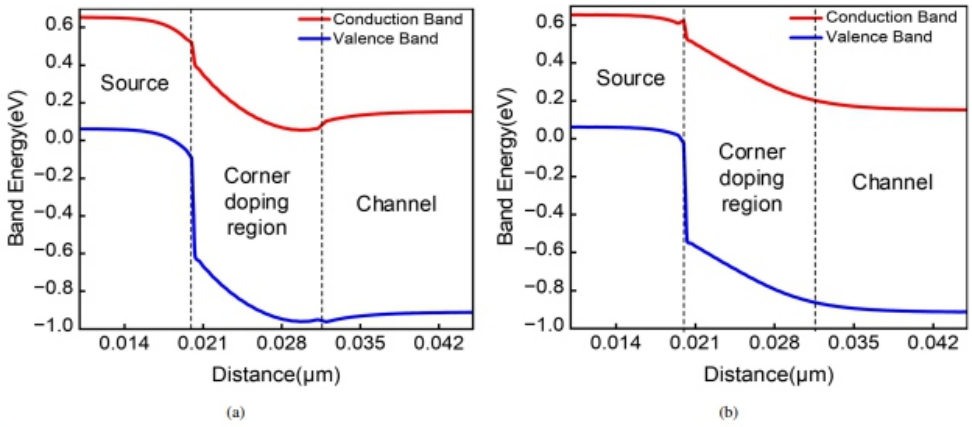


Fig. 3. Band energy diagrams (a) with and (b) without heavy doping.

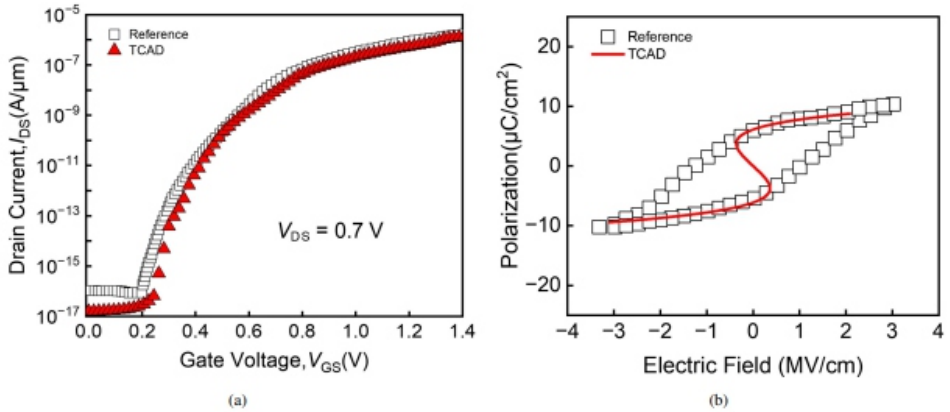


Fig. 4. (a) Calibration of the BTBT parameters using simulated transfer characteristics (I_{DS}-V_{GS}) of the referenced NCTFET [18]. (
Calibration of the L-K model matched to referenced result [25].

6.4952 × 1020 cm5 /(Fc2) and γ = 5.0 × 1030 cm9/(Fc4)[25,26]. Meanwhile, both the nonlocal BTBT model and L-K model parameters were matched to the reference [18],as shown in Fig. 4(a). Fig. 4(b) shows the simulated P-Ecurve matched to the reference data [25]. Furthermore, theoldSlotboom, Fermi, Shockley-Read-Hall recombination,High-field saturation, e-normal and doping dependencesmodels are also used. Here, the turn-on voltage (VON) wasdefined as the VGS at IDS = 2×10−13 A/μm [18]. The VTHwas extracted at IDS = 1 × 10−7 A/μm and the averagesubthreshold slope (SSAVE) was calculated by averagingthe SS in the IDS range of 2×10−13 to 1×10−7 A/μm.

Table 1. Structural parameters used for the proposed device design.

Symbol	Quantity	Value
L_G	Gate Length	71 nm
L_S	Source Length	20 nm
L_D	Drain Length	20 nm
H_D	Drain Height	28 nm
H_S	Source Height	80 nm
T_{CH}	Channel Thickness	8 nm
T_B	Barrier Thickness	4 nm

III. RESULT AND DISCUSSION

1. Channel Doping Engineering

To enhance the realizable of the simulation, we consider the actual corner shape in fabrication and replace the vertical corner with a curved corner. As shown in 5(a), electrical properties are virtually unchanged. Meanwhile, the interface defect states between the HfO2 and the channel are also taken into consideration. Acceptortype traps are added at the interface (for n-type transistors) with trap concentrations ranging from 1 × 1011 to1×1013 cm−2eV−1[27]. The transfer characteristic curvesare shown in Fig. 5(b) and curves remained almost unchanged with an increasing concentration of traps. In addition, we also consider the impact of Gaussian doping and Uniform doping of the source on transistor performance.The Gaussian doping has a peak concentration of 3×1019cm−3, a background doping of 1×1019 cm−3, and a junction depth of 6 nm as shown in Fig. 6(a). The results indicate that the curve of Gaussian doping is slightly degradedin the subthreshold region and increased in ION. This

is because as the doping concentration changes, the energyband of the source also changes. The VON decreases as thesource doping concentration increases, due to the downward bending of the energy band. The ION is determinedby the junction depth and the background concentration of

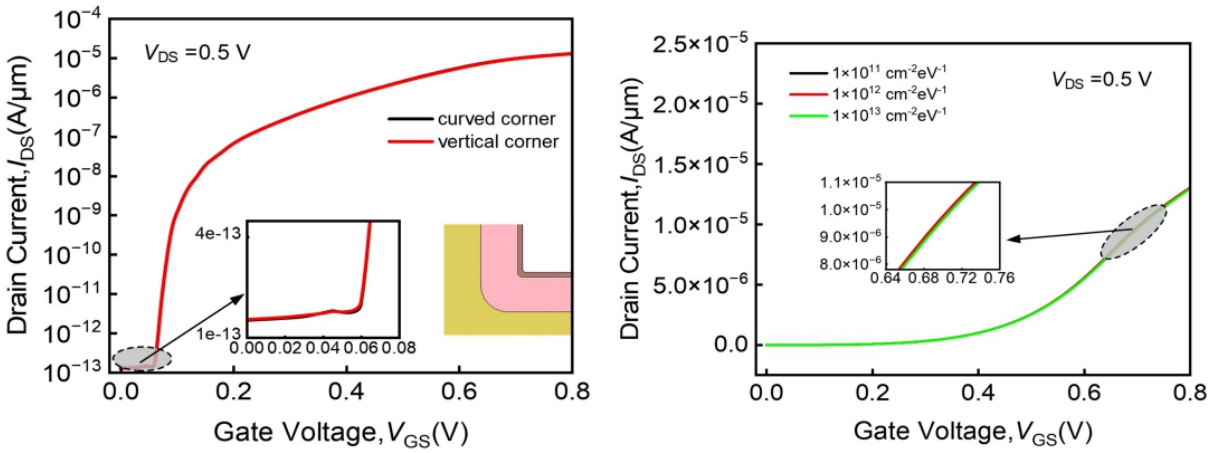


Fig. 5. (a)Transfer characteristics at V_{DS} = 0.5 V with curved corner and vertical corner. (b) Transfer characteristics at V_{DS} = 0.5 V with different acceptor-type traps concentrations.

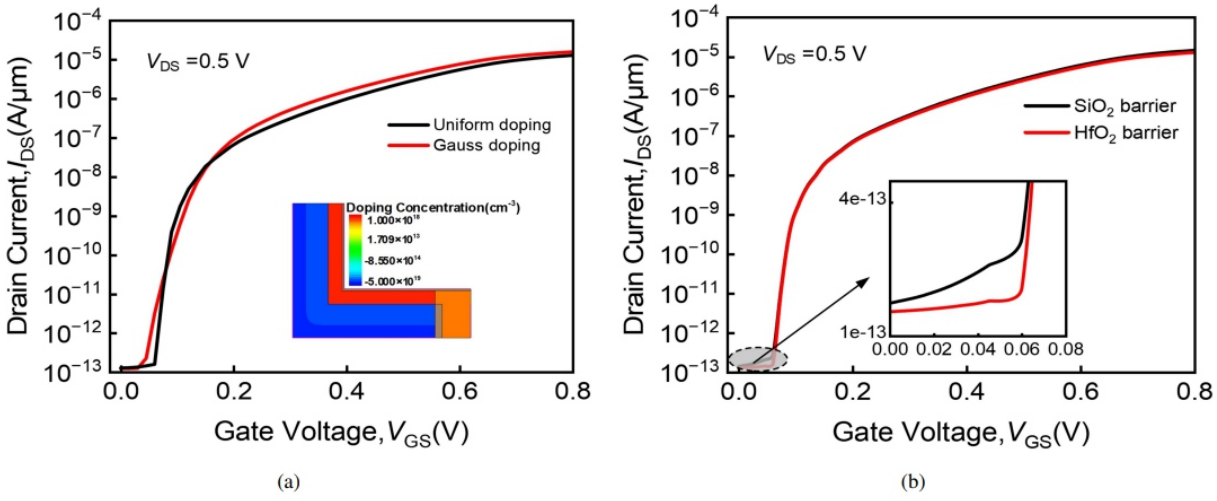


Fig. 6. (a) Transfer characteristics at V_{DS} = 0.5 V with different doping methods for source region. (b) Transfer characteristics at V_{DS} = 0.5 V with SiO_2 barrier and HfO_2 barrier.

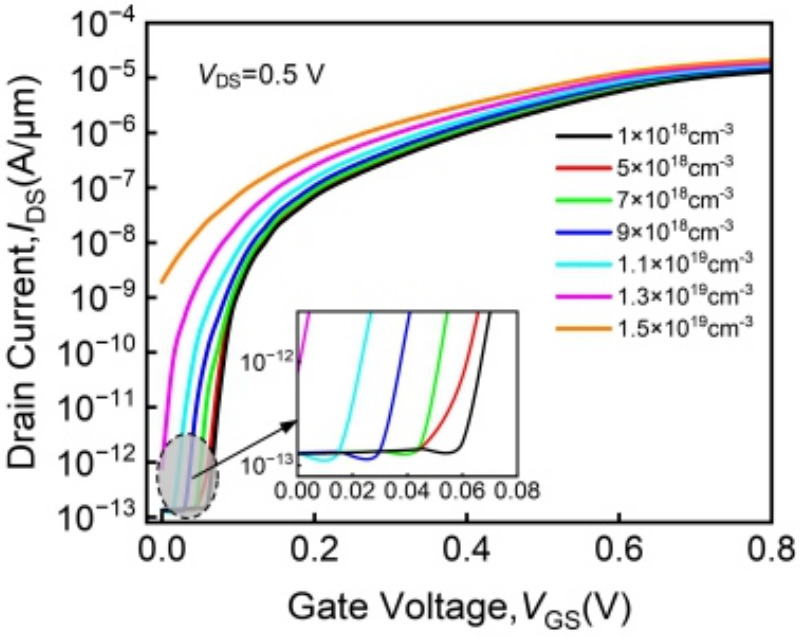


Fig. 7. Transfer characteristics at V_{DS} = 0.5 V with different $N_{CH,CO}$ values.

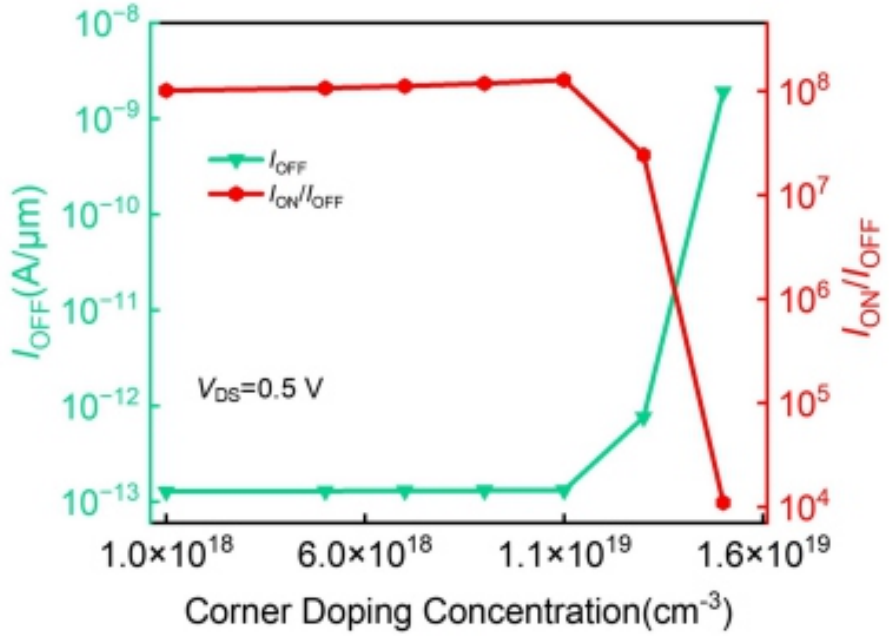
Gaussian doping. This work focuses on optimizing transistors through corner doping and the ferroelectric layer, so, in summary, we use vertical corner, no interface trap,uniformly doped transistors as the object of study.

Besides, Fig. 6(b) compares the transfer characteristic curves of using low-k material (SiO2) and using HfO2 as abarrier layer. The result shows that using HfO2 as a barrierlayer results in lower IDS at VGS below 0.06 V. Therefore,we choose to use HfO2 as our barrier layer.

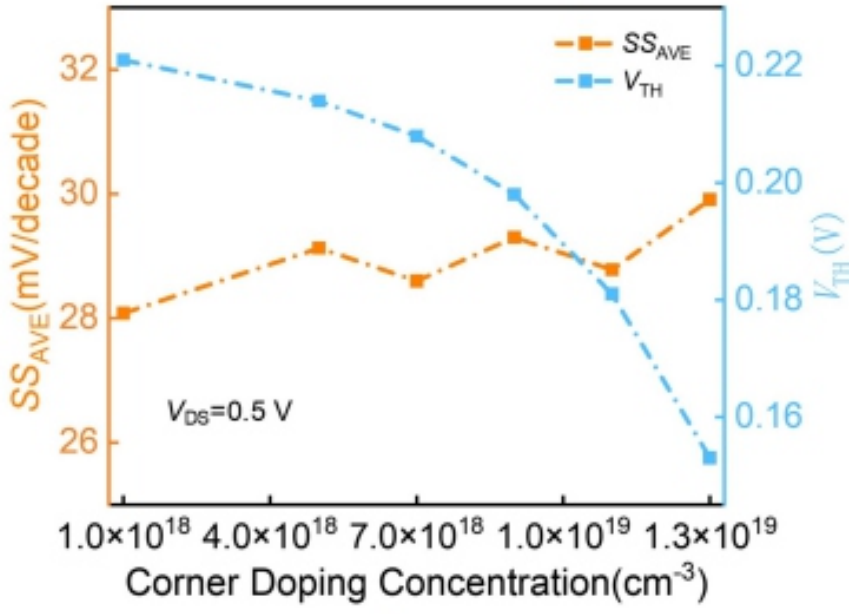
Figs. 3(a) and 3(b) indicate that heavy doping (n+- doping for an n-type TFET) can modulate the energybands of the corner doping region and reduce the tunneling barrier. To optimize the performance, the effects ofNCH,CO were assessed from 1×1018 to 1.5×1019 cm−3.

Fig. 7 shows the IDS-VGS curves of the LG-HJ-TFETwith channel doping (HJ-CD-LTFET) at different NCH,COvalues. As NCH,CO increases, the curves in the subthreshold region shift to the left, and the saturation curves moveupward. Fig. 8(a) indicates that as NCH,CO increases from1 × 1018 to 1.1 × 1019 cm−3, IOFF remains nearly constant, and ION increases, as shown in Fig. 7; thus, theswitching current ratio (ION/IOFF) increases. However, atNCH,CO = 1.3×1019 cm−3, the off-state current (IOFF) increases rapidly, and ION/IOFF decreases. The same trendis more obvious at NCH,CO = 1.5 × 1019 cm−3. Fig. 8(b)shows that VTH continuously decreases, and the rate ofreduction increases with increasing NCH,CO. Meanwhile,SSAVE remains almost unchanged when NCH,CO increasesfrom 1×1018 to 1.3×1019 cm−3.

This is because with an increase in NCH,CO, the energy bands of the corner doping region bend downwards, as



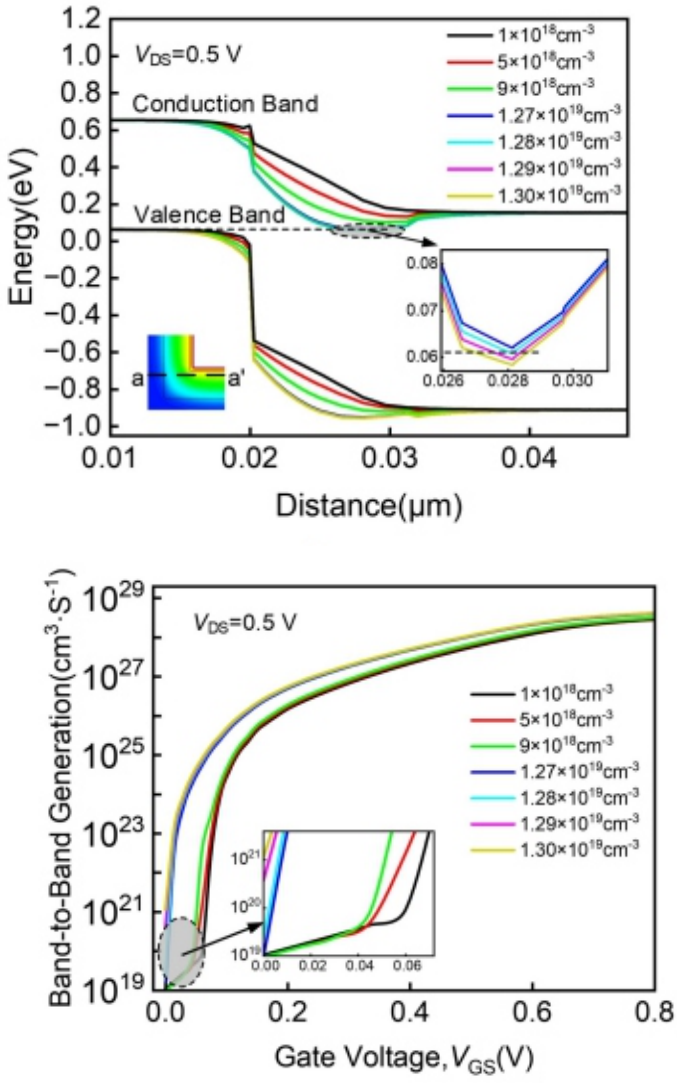
(a)



(b)

Fig. 8. (a) I_{OFF}, I_{ON}/I_{OFF}, (b) SS_{AVE}, and V_{TH} of the proposed HJ-CD-LTFET with different $N_{CH,CO}$ values.

shown in Fig. 9(a). When NCH,CO ranges from 1 × 1018 to 1.27 × 1019 cm−3, the conduction band bottom of thechannel gradually approaches the valence band top of thesource, allowing electrons to tunnel from the source tothe channel at a lower voltage. Fig. 9(b) confirms that asNCH,CO increases, significant changes in the band-to-bandgeneration increase fast at a low VGS, and the total band-toband generation is enhanced. Simultaneously, the energybands do not overlap, and the band-to-band generation remains nearly constant at VGS = 0 V. Thus, VTH and VON decrease, and ION increases. Fig. 10 shows that the BTBT inthe corner of HJ-CD-LTFET (BT BT CO) does not occur atNCH,CO from 1×1018 to 1.27×1019 cm−3. As the NCH,COcontinues to increase, the energy band continues to benddownwards and partial overlap occurs between the valence band at the top of the source and the conduction band at the bottom of the channel at VGS = 0 V, as shown in Fig. 9(a). Therefore, as indicated by Fig. 10, BT BT CO occurs



(b)

Fig. 9. (a) I_{OFF}, I_{ON}/I_{OFF}, (b) SS_{AVE}, and V_{TH} of the proposed HJ-CD-LTFET with different $N_{CH,CO}$ values.

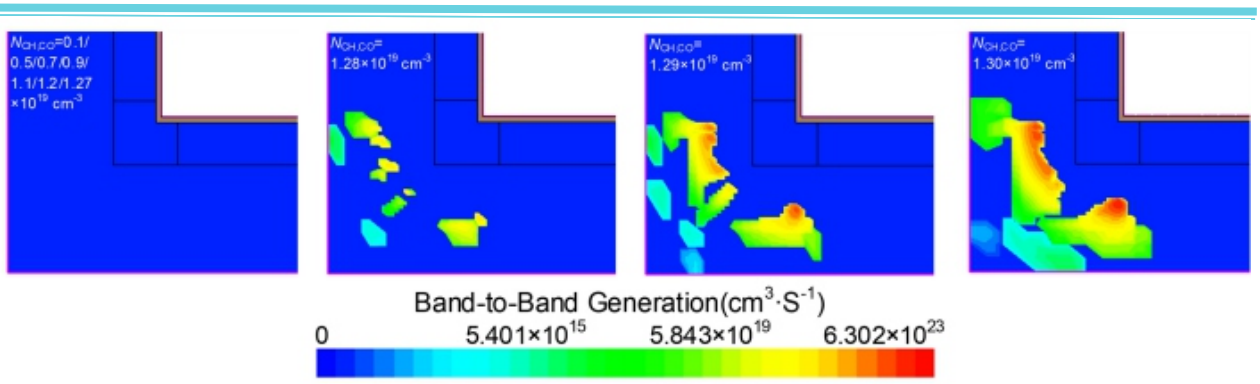


Fig. 10. BTBT diagrams at different $N_{CH,CO}$ with V_{GS} = 0 V in the corner of HJ-CD-LTFET.

to-band generation also appears a significant increase at VGS = 0 V. So, IOFF increases rapidly. Furthermore, asNCH,CO increases, the VTH and VON decrease. Therefore,SSAVE fluctuates within a certain range.

IV. FERROELECTRIC LAYER AND PARAMETER OPTIMIZATION

To further improve the device performance, a ferroelectric layer was deposited above the horizontal gate dielectric to form a negative capacitance HJ-CD-LTFET (NCHJ-CD-LTFET). Meanwhile, considering the influence of heavy doping, the effects of the ferroelectric-layerthickness (TFE) on the transistor performance were studied, with NCH,CO = 5×1018 cm−3.

Fig. 11 shows the IDS-VGS curve of the NCHJ-CDLTFETs with different TFE. When the ferroelectric-layerthickness was < 1.5 nm, the ferroelectric layer increased

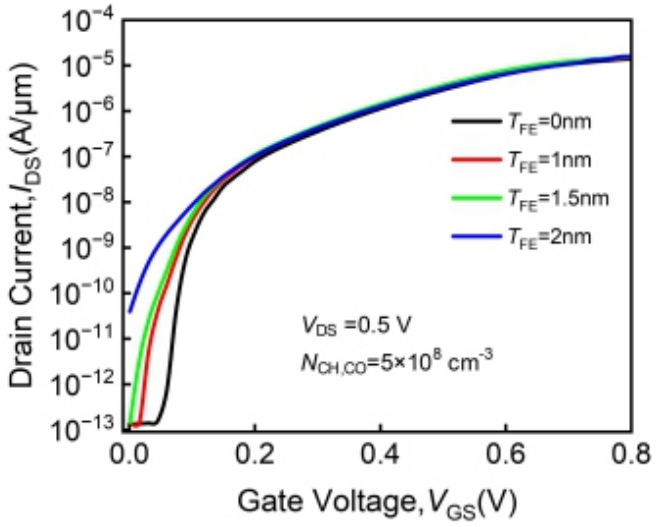


Fig. 11. Transfer characteristics at $N_{CH,CO}$ = 5 ? 10^{18} cm^{-3} with different T_{FE} values.

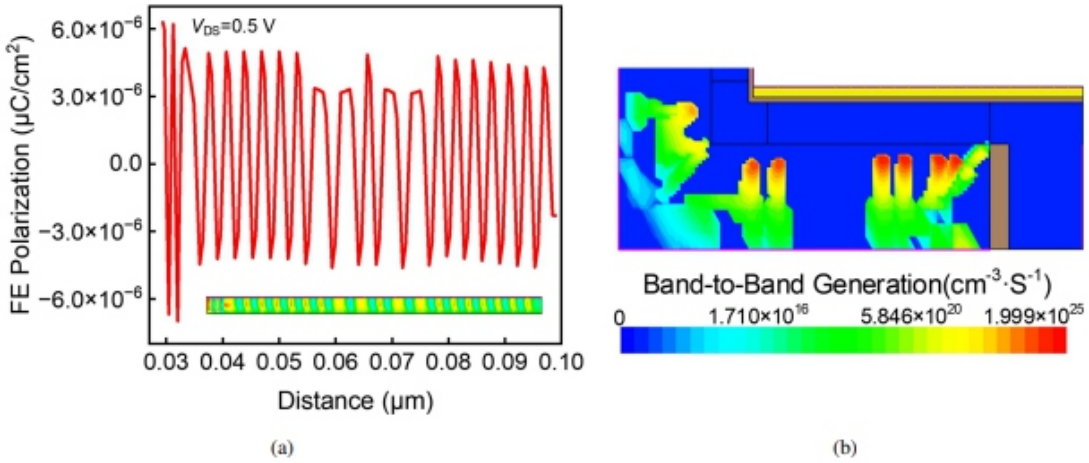


Fig. 12. (a) FE Polarization at $T_{FE} = 2$ nm. (b) BTBT diagram at $V_{DS} = 0.5$ V with $T_{FE} = 2$ nm.

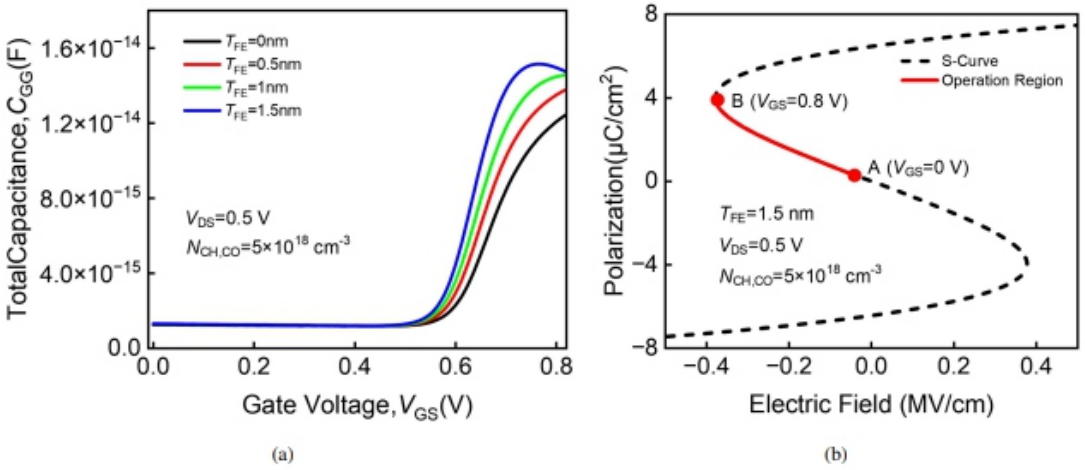


Fig. 13. (a)C_{GG} of the NCHJ-CD-LTFET at different T_{FE} values. (b) S-curve of the NCHJ-CD-LTFET and the operating region for $V_{DS} = 0.5$ V.

the internal gate voltage via negative-capacitance effects, reducingVON. However, when the ferroelectric-layer thickness was 2 nm, IOFF increased rapidly. This is becausethe polarization was unstable and fluctuated at TFE = 2 nm,as illustrated in Fig. 12(a). Fig. 12(b) shows that BTBToccurred at the polarization peak. Hence, IOFF increasedrapidly, as shown in Fig. 11.

Fig. 13(a) shows that the total capacitance (CGG) increases as the ferroelectric thickness increases, with a capacitance peak occurring at TFE = 1.5 nm, when the negative capacitance effect is most apparent [28] and no hysteresis occurs [29]. Fig. 13(b) illustrates the position ofNCHJ-CD-LTFET on the S-curve for gate voltages ranging from 0V to 0.8V. The NCHJ-CD-LTFET is operating in the negative capacitance region. Therefore, the 1.5 nm ferroelectric layer was used to investigate the impact ofvarious doping concentrations on transistor performance.

According to the above analysis, the characteristics of the NCHJ-CD-LTFET with a 1.5-nm-thick ferroelectriclayer and without a ferroelectric layer (TFE = 0 nm, HJCD-LTFET) were evaluated as

NCH,CO increased from 5 × 1018 to 1.3 × 1019 cm−3. As shown in Fig. 14(a),when the doping concentration was 5×1018 and 9×1018cm−3, the VON with the ferroelectric layer was lower thanthat at TFE = 0 nm. However, CGG remains essentiallyunchanged as NCH,CO increases as shown in Fig. 14(b).In addition, Fig. 15(a) shows that the VTH of the NCHJCD-LTFET was lower than that without the ferroelectric

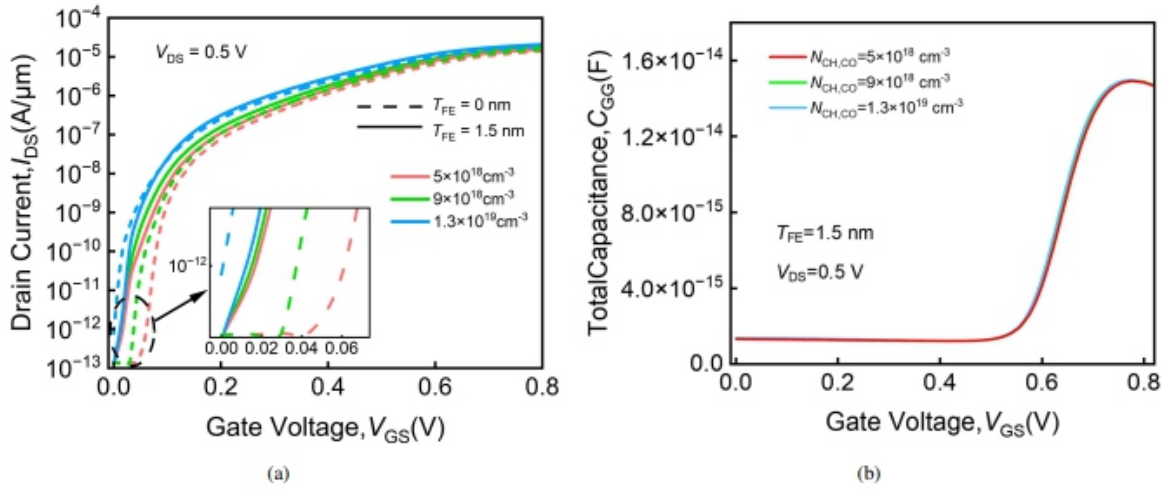


Fig. 14. (a) Transfer characteristics of the NCHJ-CD-LTFET with different values of T_{FE} and $N_{CH,CO}$. (b) C_{GG} of the NCHJ-CD-LTFET at different $N_{CH,CO}$ values.

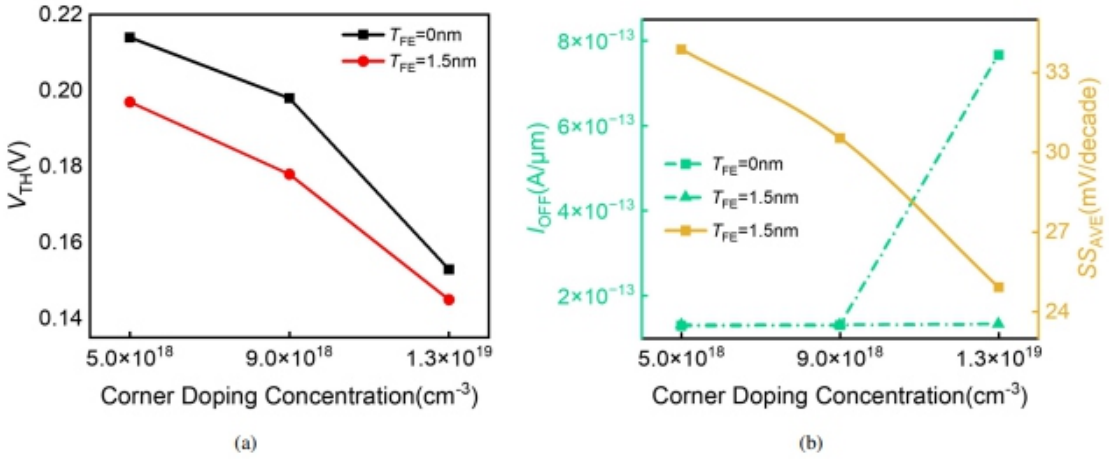


Fig. 15. (a) V_{TH} of the NCHJ-CD-LTFET with different values of T_{FE} and $N_{CH,CO}$. (b) I_{OFF} of the NCHJ-CD-LTFET with different values of T_{FE} and $N_{CH,CO}$, and SS_{AVE} of the NCHJ-CD-LTFET with different values of $N_{CH,CO}$ at T_{FE} = 1.5 nm.

layer. As shown in Fig. 15(b), SSAVE decreases with an increase in NCH,CO at TFE = 1.5 nm. In particular, whenNCH,CO was 1.3×1019 cm−3, IOFF with a 1.5-nm-thick ferroelectric layer decreased significantly, as shown in Fig.15(b). This is because owing to the negative-capacitanceeffects, the ferroelectric layer amplified the internal gatevoltage, increasing in channel surface potential, reducingVTH. Simultaneously, some electrons that could not initially tunnel in the subthreshold region

could tunnel from the source to the channel. Thus, SSAVE decreased. WhenNCH,CO was 1.3×1019 cm−3, the ferroelectric layer inhibited the tunneling of overlapping bands owing to heavydoping. As shown in Fig. 16(a), compared with the transistor without a ferroelectric layer, no electrons tunneled in the corner for the NCHJ-CD-LTFET at VGS = 0 V and VDS = 0.5 V.

Finally, the thickness of the ferroelectric layer and doping concentration of the corner doping region were adjusted to improve the electrical characteristics of the transistor, as shown in Fig. 16(b). Table 2 presents the key performance parameters of the LG-HJ-TFET, HJ-CD-LTFETand NCHJ-CD-LTFET

V. CONCLUSION

An NCHJ-CD-LTFET was developed on the basis of the L-shaped-gate TFET and analyzed using TCAD simulations. In contrast to the LG-HJ-TFET, channel doping

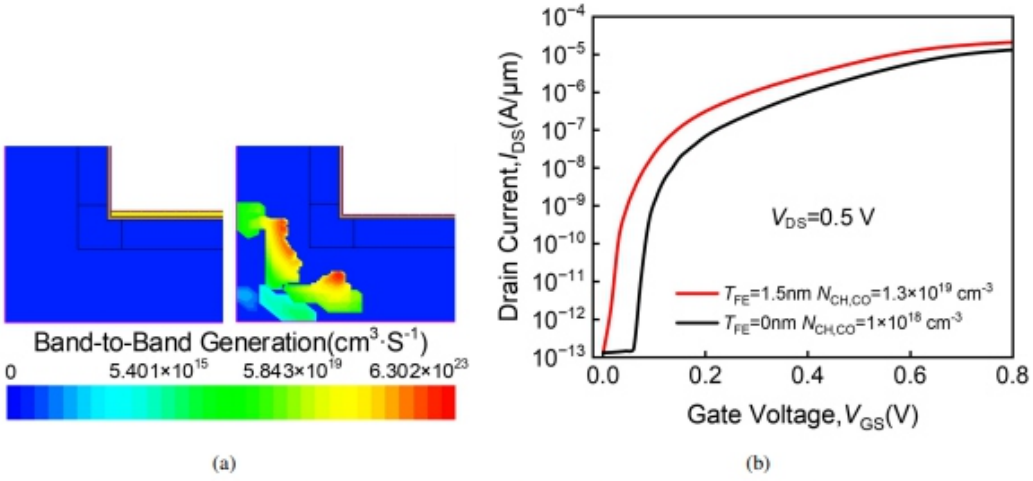


Fig. 16. (a) BTBT diagrams at $N_{CH,CO} = 1.3 \times 10^{19}$ cm^{-3} with $T_{FE} = 1.5$ nm and without the ferroelectric layer. (b) Transfer characteristics of the NCHJ-CD-LTFET and LG-HJ-TFET at $V_{DS} = 0.5$ V.

Table 2. Key parameters of the LG-HJ-TFET, HJ-CD-LTFET and NCHJ-CD-LTFET.

	LG-HJ-TFET	HJ-CD-LTFET	NCHJ-CD-LTFET
I_{ON} (μA/μm)	13.02	16.87	20.58
I_{ON}/I_{OFF}	1.016×10^8	1.282×10^8	1.555×10^8
V_{TH} (V)	0.221	0.180	0.145
SS_{AVE} (mV/decade)	28.08	28.78	24.92

can modulate the energy bands, narrowing the bandgap between the source and channel, and reducing the threshold voltage. Meanwhile, regulating the ferroelectric-layerthickness via heavy doping can further improve the electrical performance. In particular, when the bandsoverlap in the corner doping region at NCH,CO = 1.3×1019cm−3 with VGS = 0 V, the ferroelectric layer can reduce IOFF and the power consumption through negativecapacitance effects. Adjusting the doping concentration of the

channel corner region and the thickness of the ferroelectric layer increased the ION and ION/IOFF of the NCHJCD-LTFET by 58% and 53%, respectively, and reduced VTH and SSAVE by 34% and 11%, respectively.

ACKNOWLEDGEMENT

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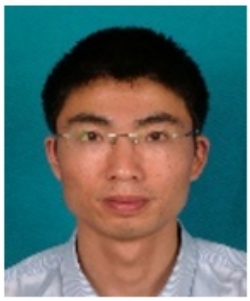

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